Gain Insights of MIPI D-/M-/C-/A-PHY into Best Design/Testing

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Solutions Engineer / Keysight Technologies	

Agenda

- MIPI PHY spec timing updating
- PHY testing updating and solution
  - ✓ M-PHY
  - ✓ D-PHY
  - ✓ C-PHY
  - ✓ A-PHY
- Probing with MIPI Signals
- Q&A

Roadmap by MIPI Alliance

SPECIFICATION AND CTS TIMING

mipi DEVCON

		CTS	Adopted	2021 Q4	2022 Q1	Q2	Q3	Q4	2023 Q1	Q2	Q3	Q4	
A-PHY		✔	07 SEP 2020 1.0	1.1									v1.0 @ ~16 Gbps/lane
C-PHY		✔	21 JUL 2021 2.1										v2.0 @ 6Gsps
D-PHY		✔	21 JUL 2021 3.0				3.5						v3.0 @ 9 Gbps
M-PHY		✔	29 SEP 2021 5.0										v5.0 @ 23.32Gbps
IPC (M-PHY)													
UniPro		✔	11 JAN 2018 1.8		2.0								Unified Protocol for UniPort-M

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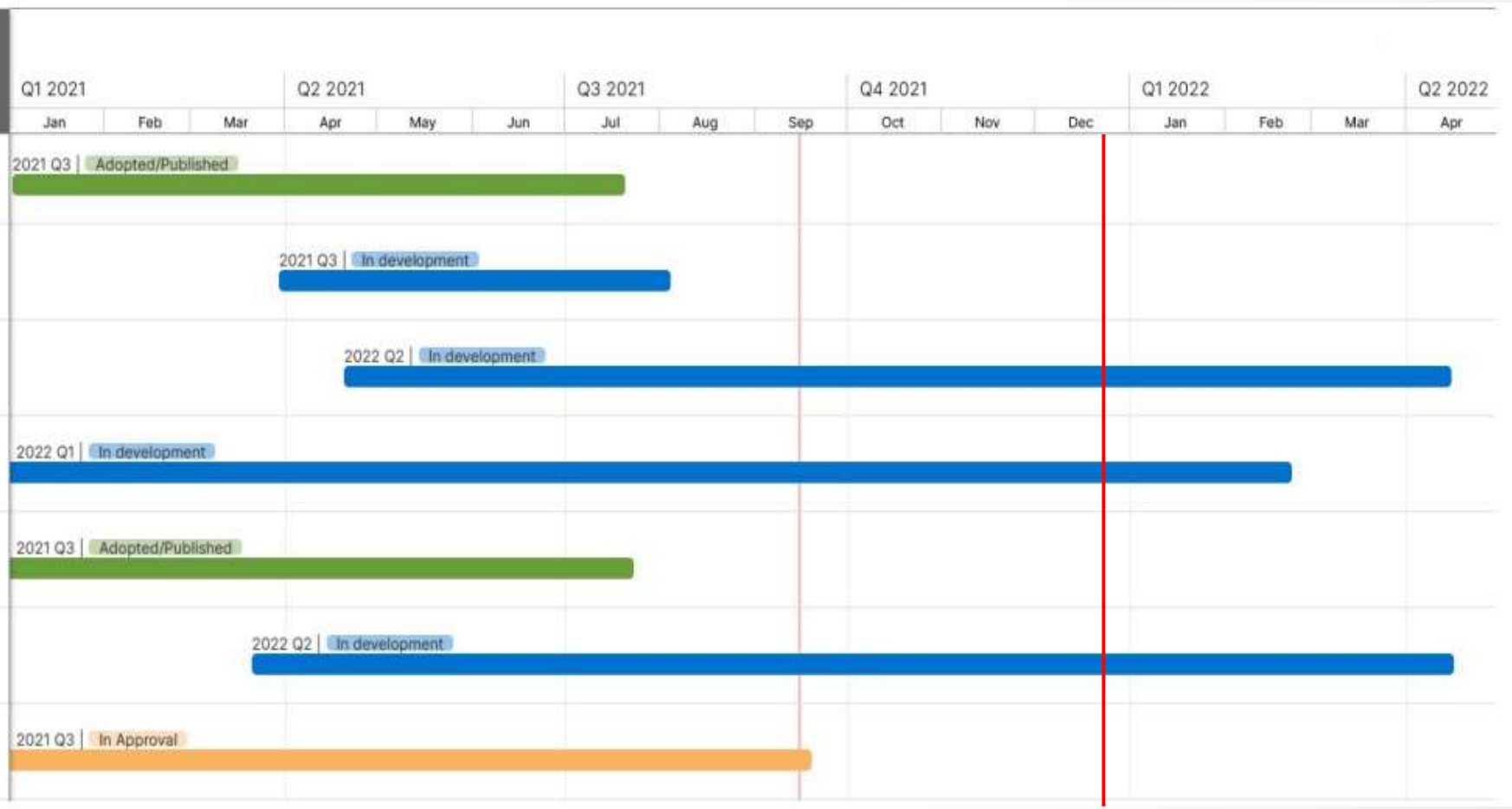
C/D/M PHY WG

Workspace line	Release name	Adopted Version
PHY	C-PHY v2.1	v2.1
	CTS for C-PHY v2.1	v2.1
	CTS for D-PHY v3.0	v3.0
	CTS for M-PHY v5.0	v4.1
	D-PHY v3.0	v3.0
	D-PHY v3.5	v3.0
	M-PHY v5.0	v4.1



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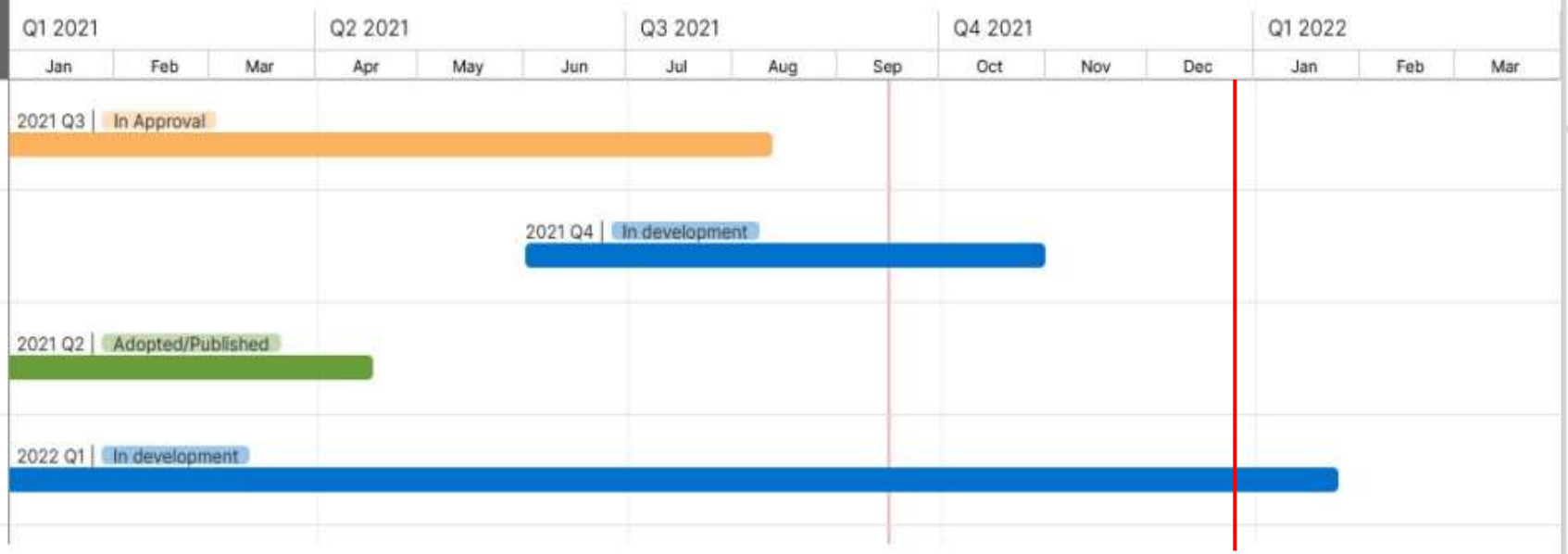
Event timing

KMF timing

A-PHY WG

Workspace line	Release name	Adopted Version
A-PHY WG	A-PHY v1.1	v1.0
	AppNote #2 for A-PHY v1.0: Re-training and Re-transmission	v1.0
	AppNote for A-PHY v1.0 - Profile 1 & Profile 2	v1.0
	CTS for A-PHY v1.0	v1.0



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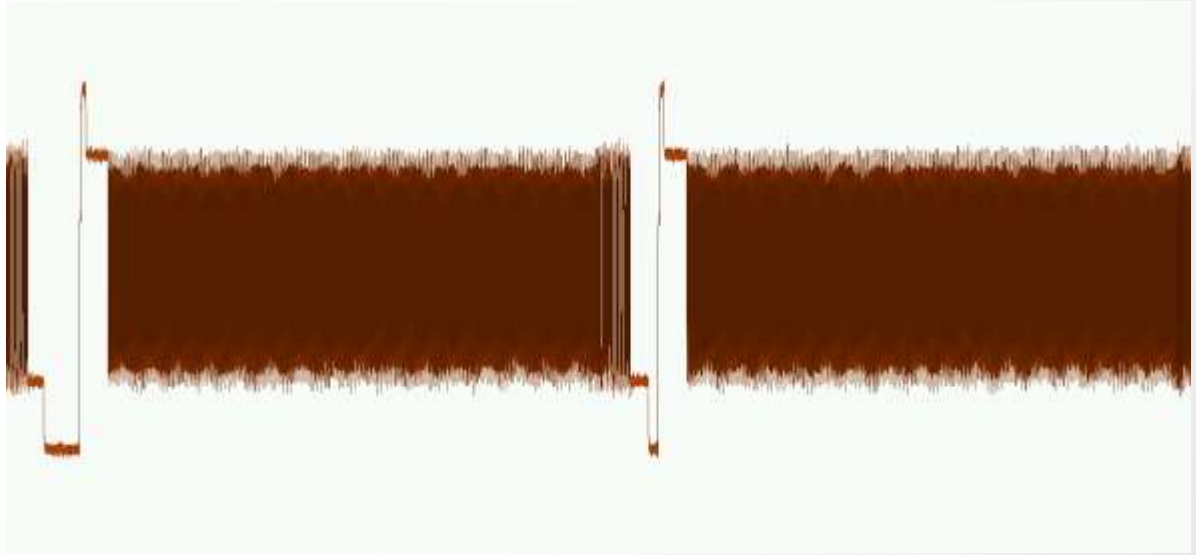
MPHY updating and solution



M-PHY Specification update

VERSION 4.0 TO 4.1

M-PHY 4.0 : Approved Aug 3, 2015

M-PHY 4.1 : Approved Mar 28, 2017

- Minor spec clarification
- Target BER 10^{-10} to 10^{-12}

M-PHY Specification update

VERSION 4.1 TO 5.0

M-PHY 4.2.1 : Approved Mar 28, 2017

M-PHY 5.0 : Approved Sep 29, 2021

- Adding HS Gear 5 speed
- HS data rate of Gear 1 ~ Gear 4 adjustment
- PWM – G1 mandatory only

M-PHY CTS updates

VERSION 3.1 TO 4.1

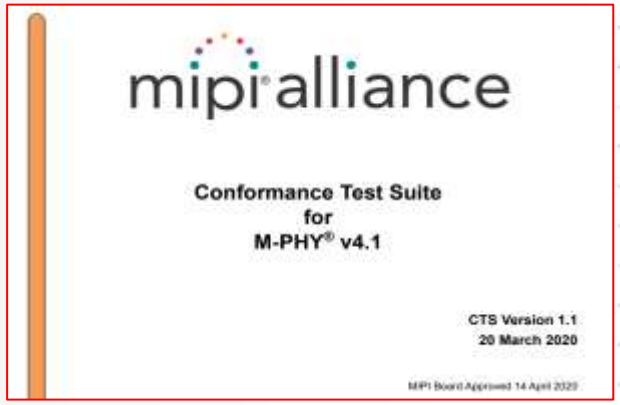
CTS 3.1 : On-going(revision 21)

CTS 4.1 : Approved April 4, 2020

- Test 1.1.7 – HS-TX G3 and G4 Differential AC Eye (TEYE-HS-G3/G4-TX, VDIF-AC-HS-G3/G4-TX)
- Minor updates

M-PHY CTS updates

VERSION 4.1 TO 5.0 DRAFT



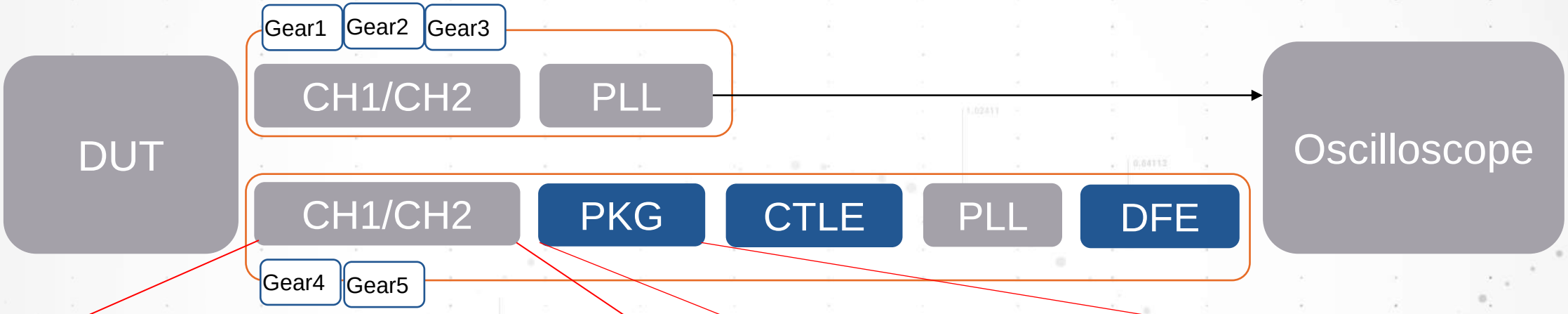
CTS 4.1 : Approved April 4, 2020

CTS 5.0 : On-going(R0.2)

- CTS update to support MIPI MPHY G5
- Adding HS/PWM/SYS TX for HS-G5
- Adding S parameter/impedance tests for HS-G5

MIPI M-PHY Embedding Channel + Package Model

NEW REFERENCE PACKAGE MODEL



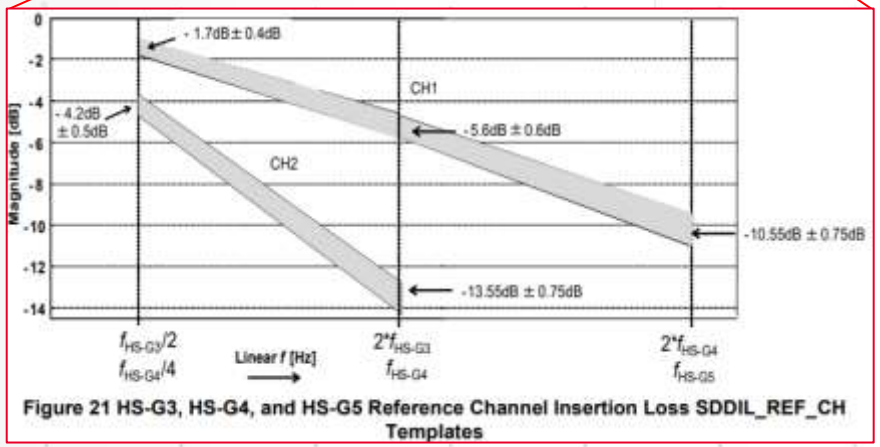
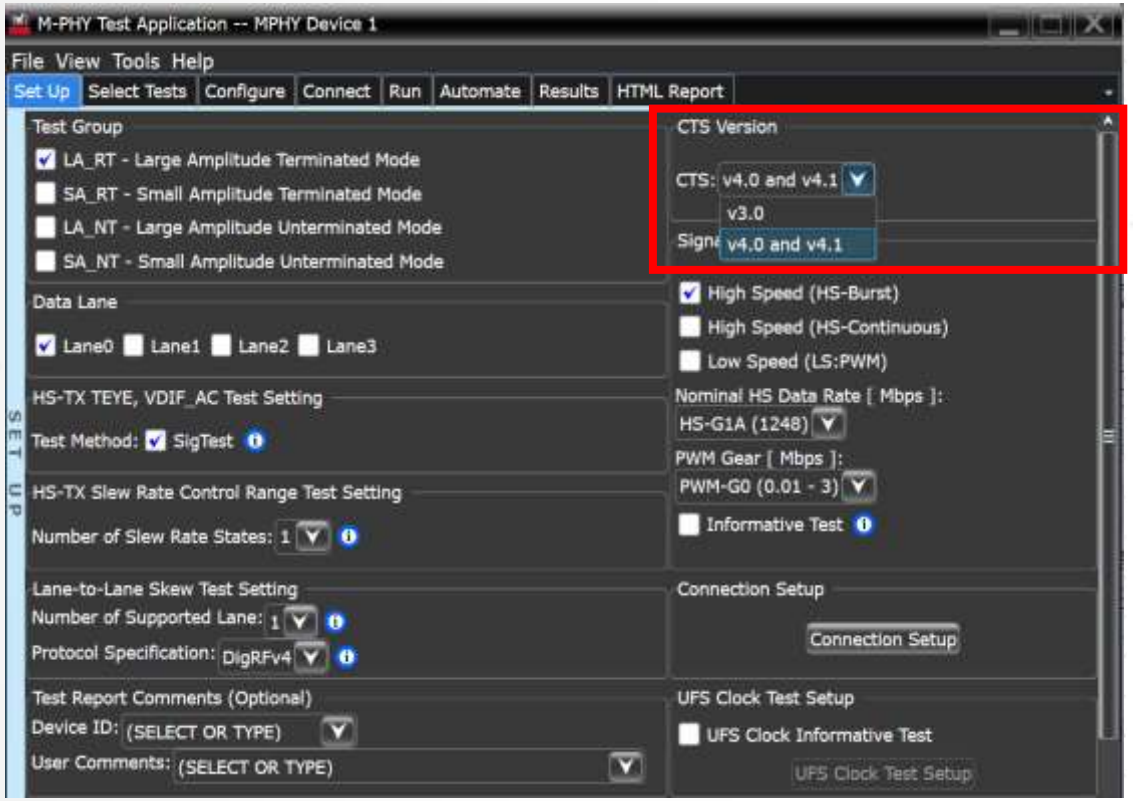


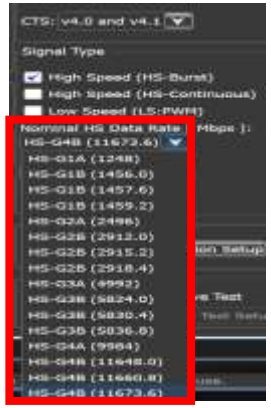
Figure 21 HS-G3, HS-G4, and HS-G5 Reference Channel Insertion Loss SDDIL_REF_CH Templates

Figure 27 HS-G4 Reference Package Insertion Loss Information

D9040MPHC MIPI M-PHY Tx test solution

SUPPORTING GEAR4 TEST AND UP TO GEAR5 SOON





Added support for the following HS-G4 Data Rate to support CTS “v4.0 and v4.1”.

- HS-G4A (9984)
- HS-G4B (11648.0)
- HS-G4B (11660.8)
- HS-G4B (11673.6)

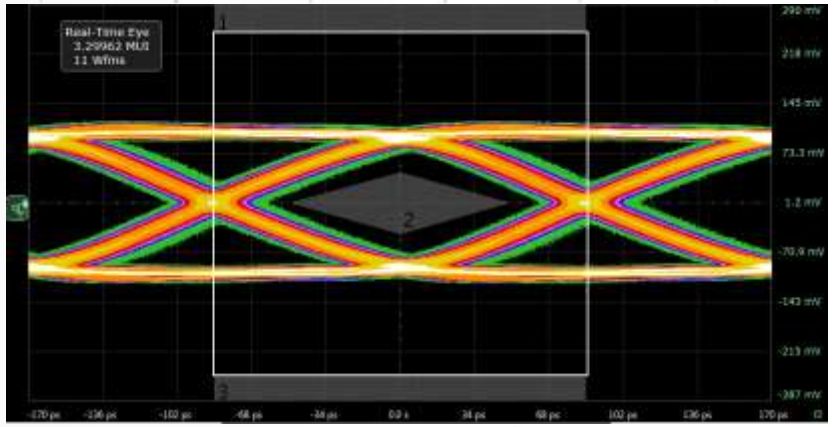
Added configurable option of “SigTest” (with remote name of “TEYESigTestEnable”) in Set Up tab.
This configurable option is used to enable or disable Test 1.1.7 TEYE_G4, VDIF_AC_G4 [SigTest] tests.

Note: It is the same Sig-Test using in G5 speed

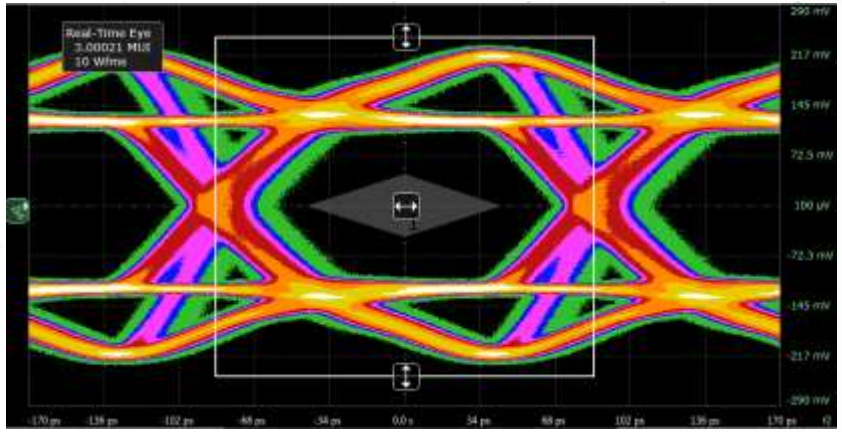
Keysight D9040MPHC M-PHY Tx test software

TEST RESULT EXAMPLE

1.1.7 – TEYE_G3_LA_RT_TX(CH2 embedded)

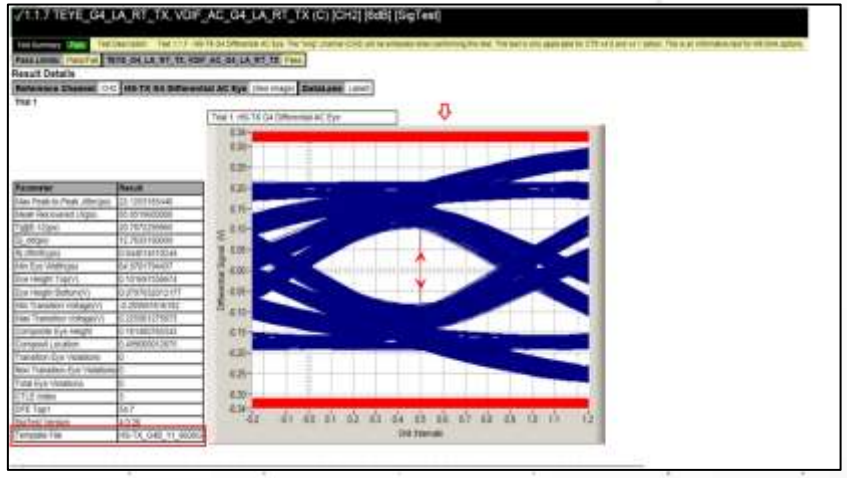


1.1.7 – TEYE_G3_LA_RT_TX[Far End HS-RX test point]



1.1.15 – TJ_LA_RT_TX

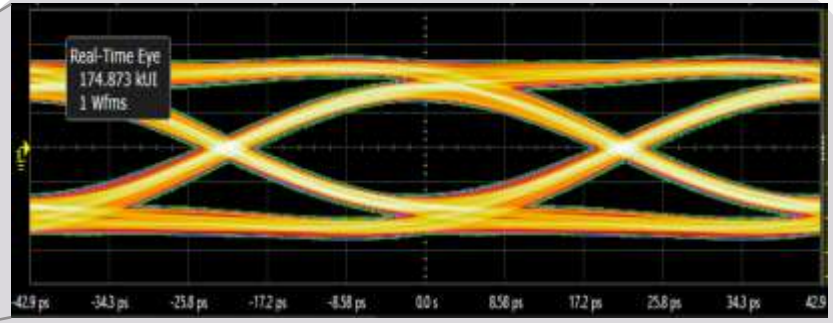
1.1.7 – TEYE_G4_LA_RT_TX(SigTest tool embedded)



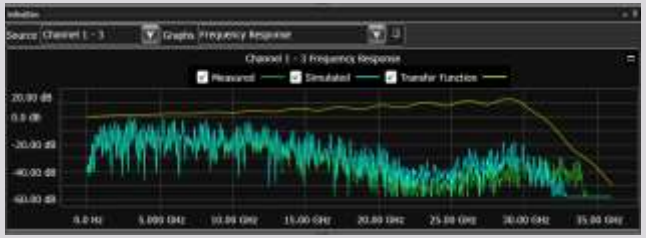
MIPI MPHY Gear 5 testing with UXR

50G BANDWIDTH; MAXIMUM SAMPLE RATE 256G

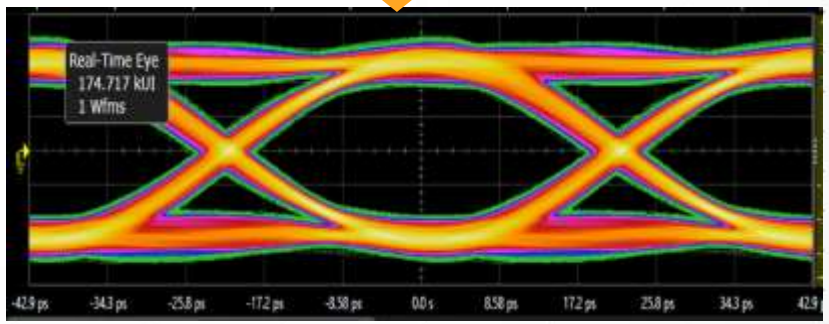
Testing tool of M-PHY Gear 5 is Sig-Test the same as Gear 4 and not released yet



Original



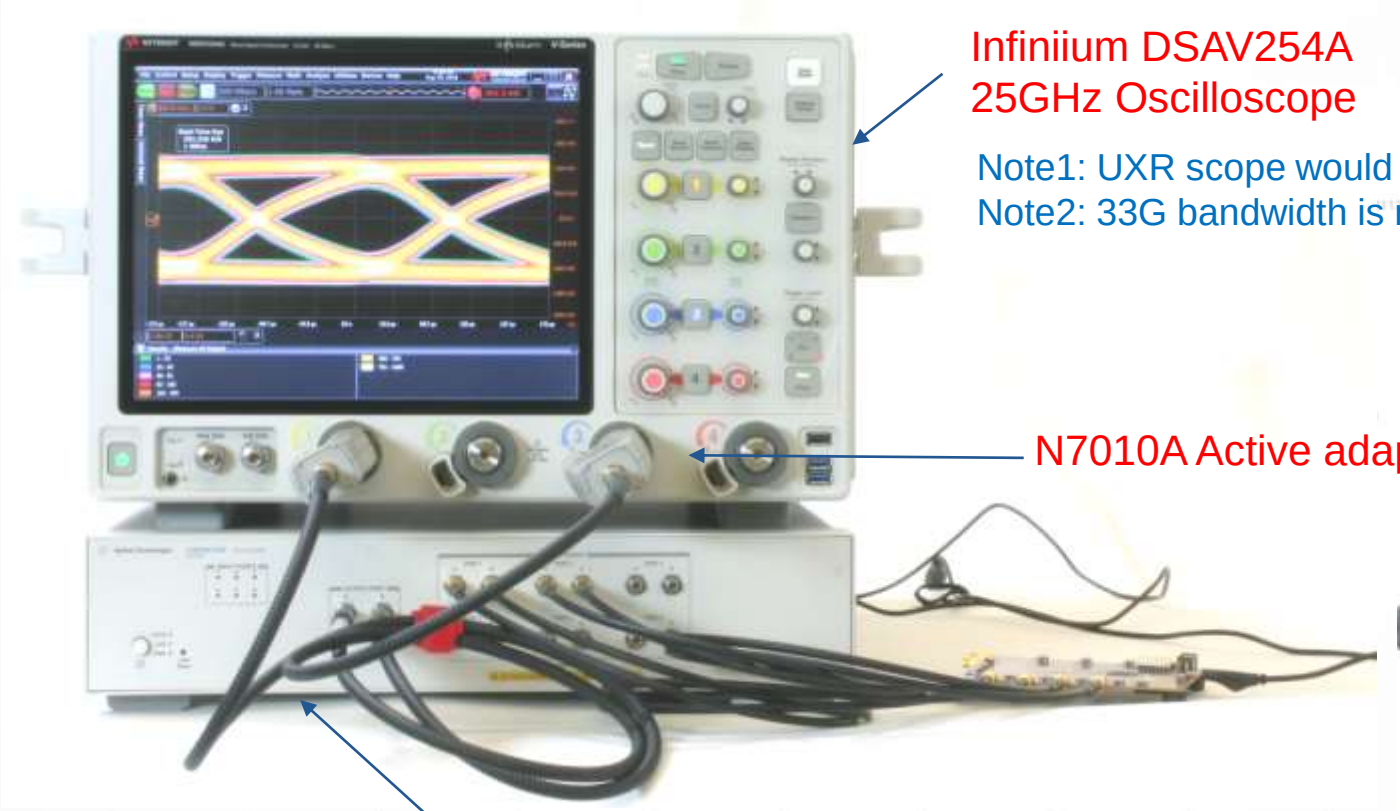
De-embedding



Simulated

M-PHY Typical TX Setup

- Simplified TX setup with N7010A active termination adaptor



Infiniium DSAV254A
25GHz Oscilloscope

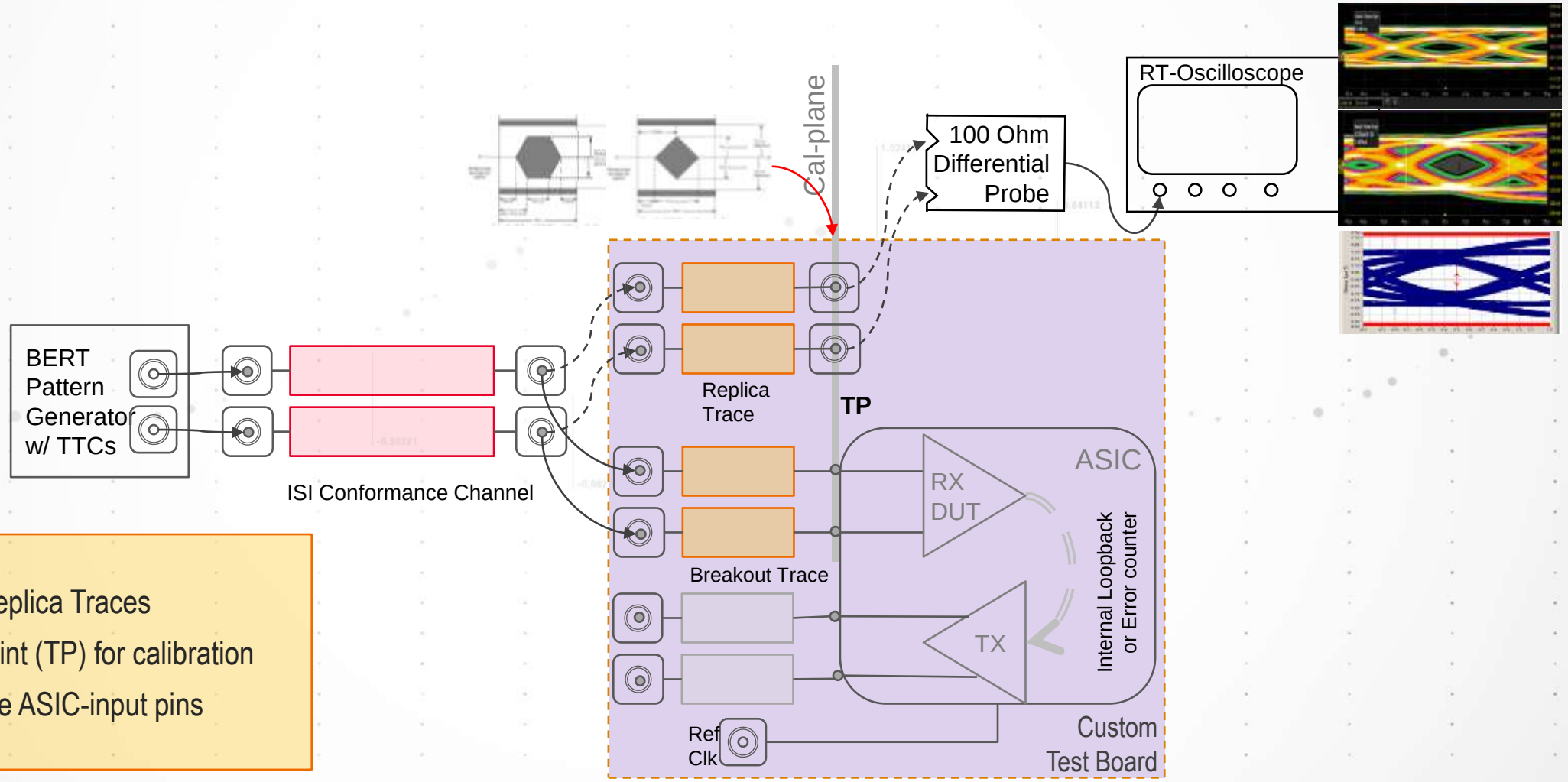
Note1: UXR scope would be better choice for higher speed
Note2: 33G bandwidth is necessary for G5(not finalizing yet)

N7010A Active adaptor

2x6 (1x6 differential) Switch
Matrix Keysight U3020AS26
(for multi lane testing; optional)

M-PHY G1~G4 RX Test and Calibration

STRESS SIGNAL GENERATION AND CALIBRATION ACCORDING TO CTS



Test board with Replica Traces

- creating test point (TP) for calibration
- equivalent to the ASIC-input pins

M-PHY Gear5 Frame Generator

MIPI M-PHY N5991 Frame Generator

CONNECTION SIGNAL ABOUT

Connection Setup

BERT

Initialize on connect

Offline Connection

Instrument: M8040A

Channels: 1

M8040A Advanced Simple

Host IP address: 127.0.0.1

Hislip: inst0

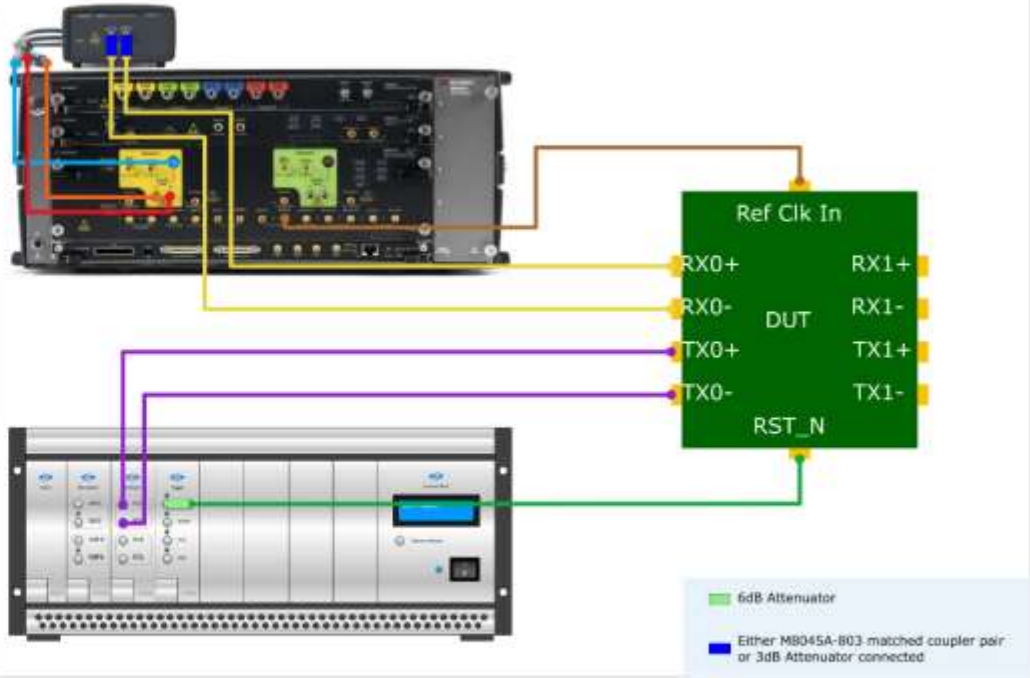
M8040A Configuration

Low speed analyzer (DSGA):

DSGA Trigger:

DSGA address TCPIP0::127.0.0.1::5025::SOCKET

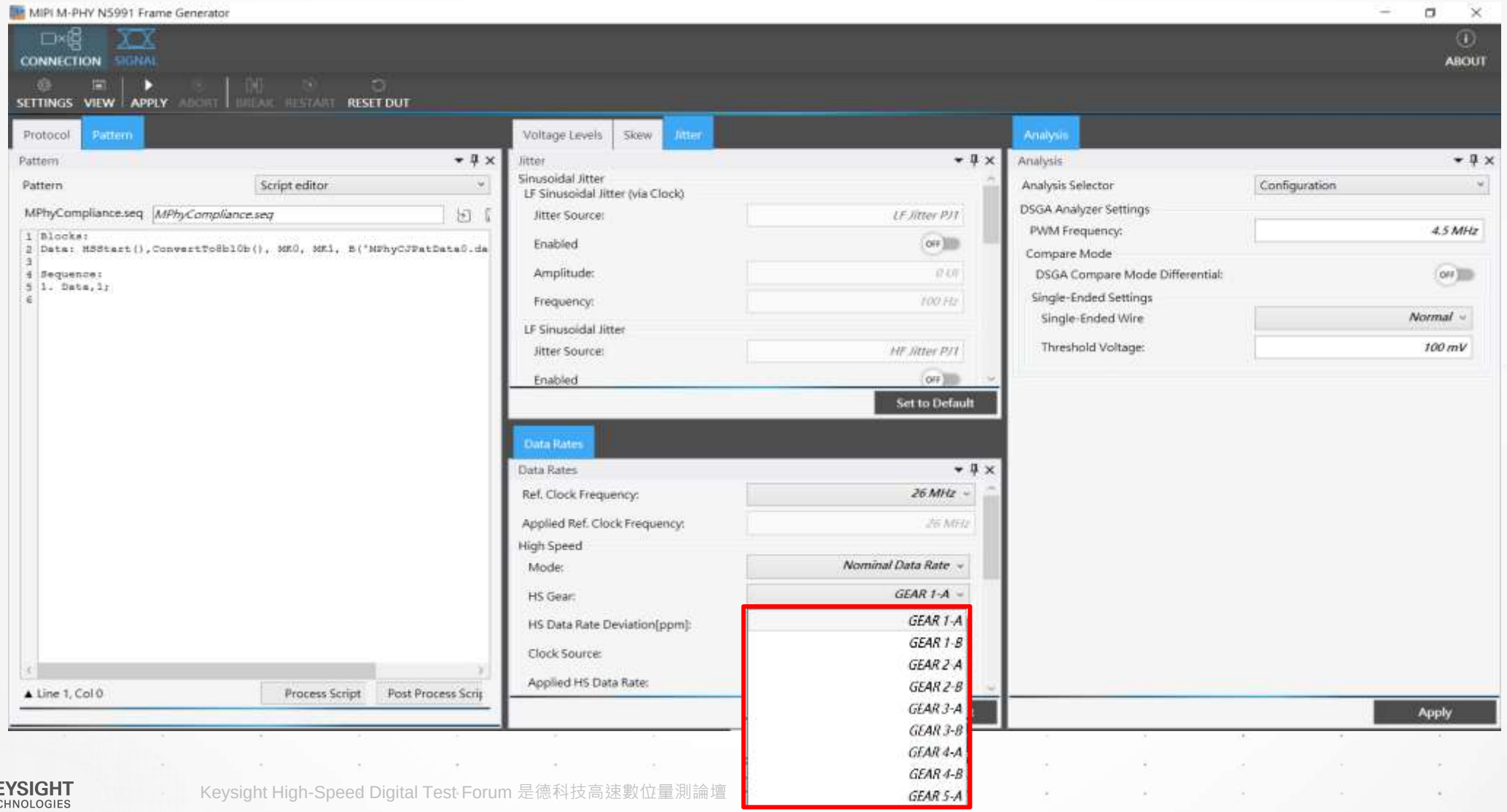
Use Calibrations:



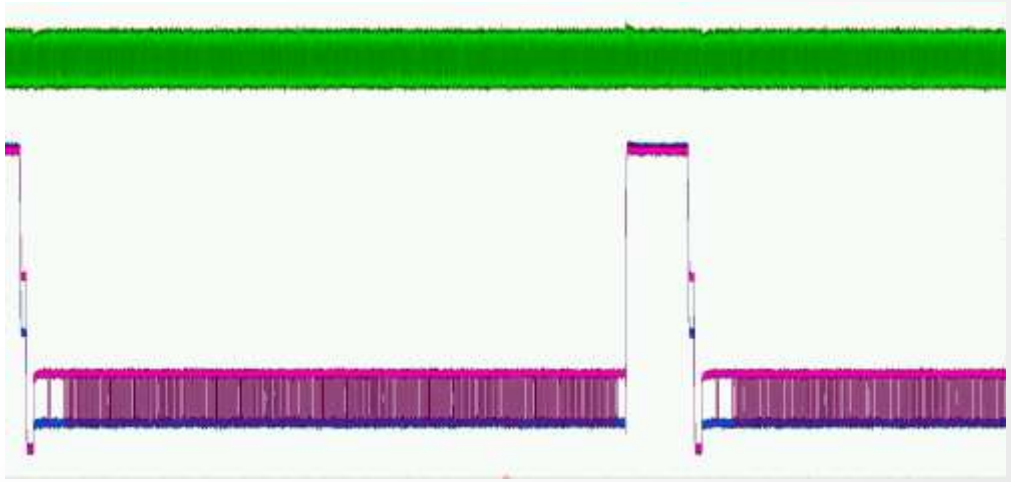
- Connect the Data0 output of J-BERT to either M8045A-803 Power Divider or 3dB Attenuator and then connect to the test fixture of the DUT.
- Connect the Trig Out Complement output of the J-BERT to the Ref. Clock Input of the DUT.
- Connect the First Trigger Out of the DSGA to the 6dB Attenuator and then to the Reset In of the DUT
- Connect the Tx of the test fixture of the DUT to the First Analyzer of DSGA.
- Note: When M8045A-803 Power Divider is used, terminate its above output

Connect Disconnect

M-PHY Gear5 Frame Generator



DPHY updating and solution



Specification updates in MIPI D-PHY

D-PHY 2.0 : Approved Mar 8, 2016

D-PHY 2.1 : Approved Mar 28, 2017

- Up to 6500Mbps with Short reference channel (8K support)
- Lower LP voltage level from 1.2V to 1V
- HS-Idle (lower latency)
- Programmable Preamble(RX PVT calibration due to LP signal)

Specification updates in MIPI D-PHY

D-PHY V2.5 IS APPROVED

D-PHY 2.1 : Approved Mar 28, 2017

D-PHY 2.5 : October 17, 2019

- ALP(Alternate Low Power)
- Fast Line turnaround
- IoT Application support
- PPI (PHY-Protocol Interface) update

Specification updates in MIPI D-PHY

D-PHY V3.0 IS ONGOING

D-PHY 2.5 : October 17, 2019

D-PHY 3.0 : July 21, 2021

- Data rate increase : 9Gbps – 12Gbps
- DDR Clock
- RX equalizer(1st order CTLE)

CTS updates in MIPI D-PHY

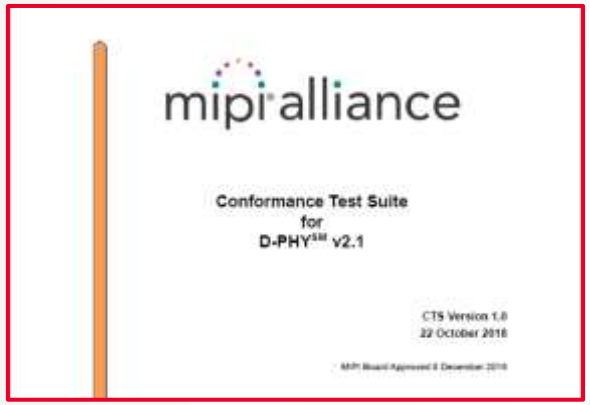
CTS 1.2 : April 24, 2017

CTS 2.1 : October 22, 2018

- Test 1.5.7 – HS-TX Data and Clock Eye Diagram
- Test 1.4.19 – TX Spread Spectrum Clocking(SSC) Requirement
- Test 1.4.18 - Clock Lane HS Clock Delta UI(new method)
- Test 1.4.20 - Clock lane HS Clock Period Jitter
- Test 1.5.9 - Alternate Calibration Sequence
- Test 1.5.10 - Preamble Sequence

CTS updates in MIPI D-PHY

NO D-PHY V2.5 CTS



CTS 2.1 : October 22, 2018

N/A

CTS 3.0 : 2H of 2022(estimated)

- No CTS in D-PHY2.5 spec
- It would be the same as C-PHY, Data and Clock eye diagram need to be updates to use Equalization.

ALP(Alternate Low Power)

REPLACE LEGACY LP

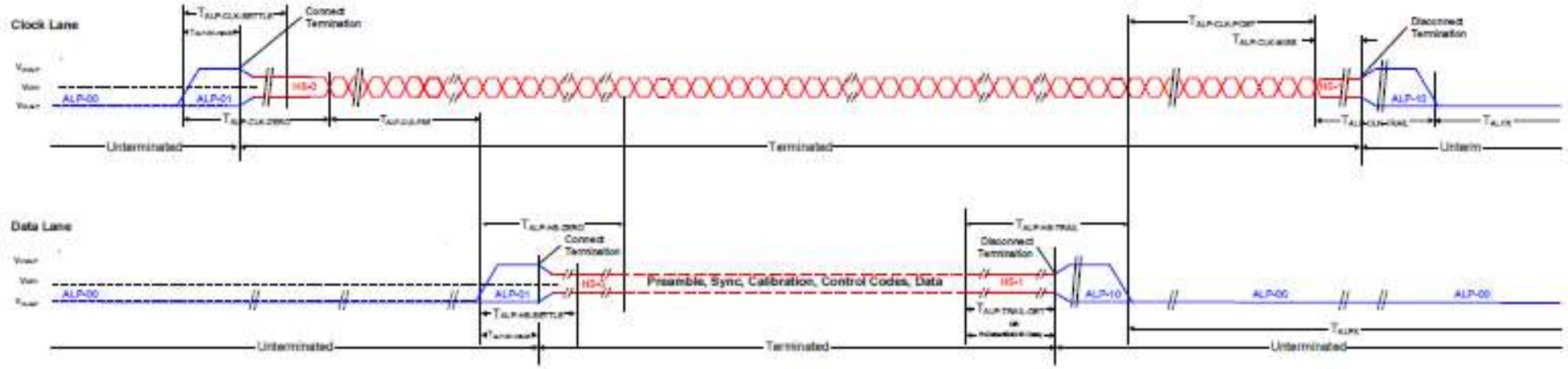


Figure 17 ALP Mode General Burst Format

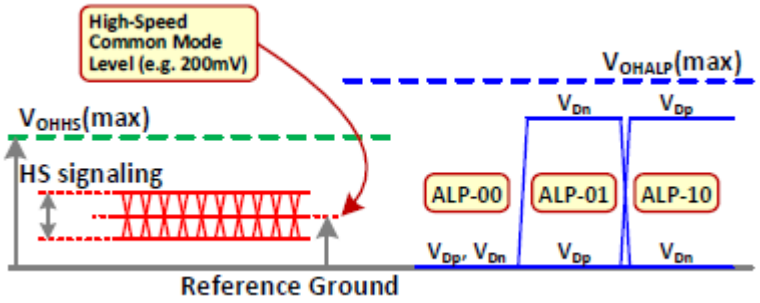
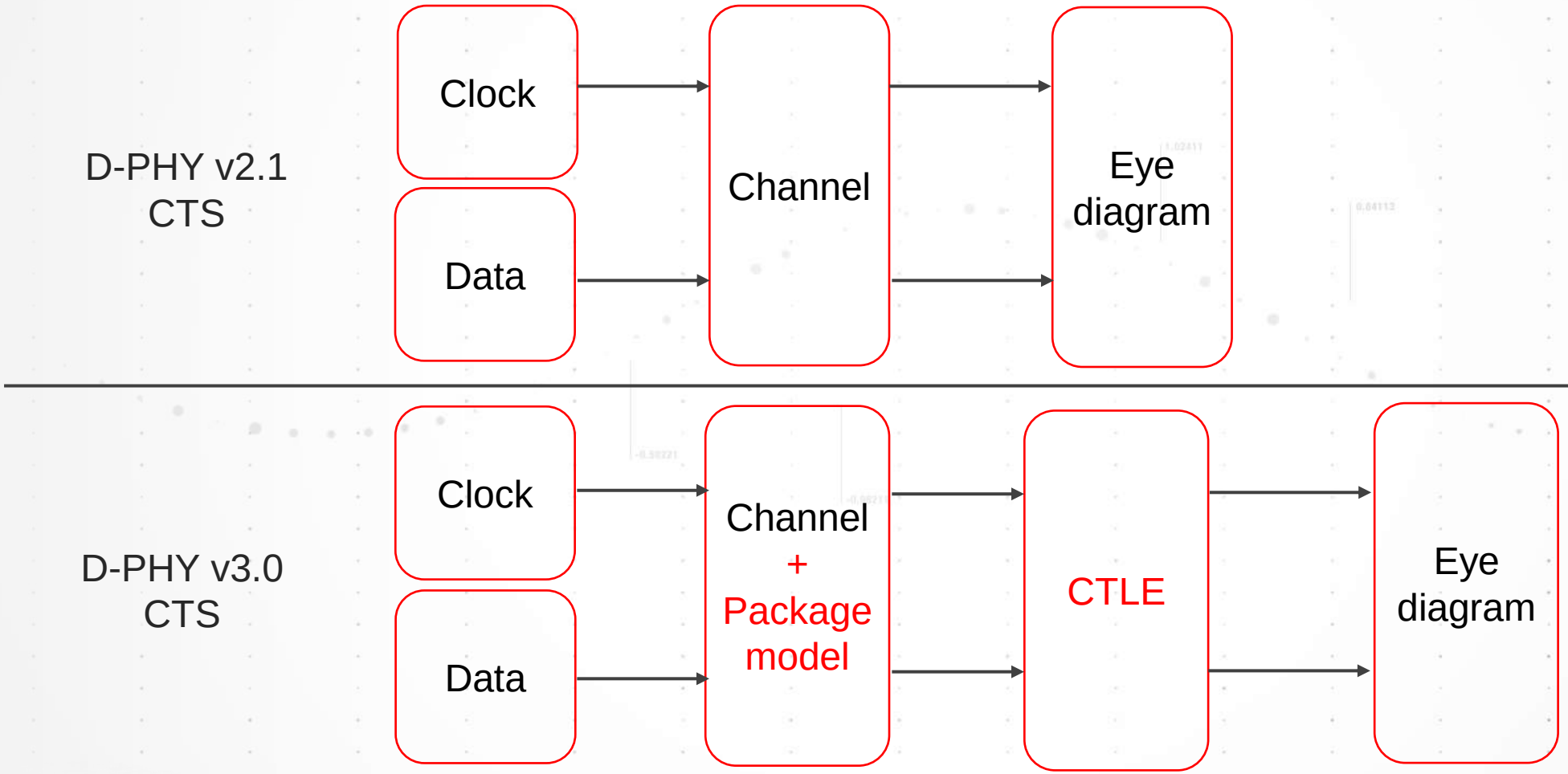


Table 3 ALP Mode Lane State Descriptions

State Code	Line Voltage Levels		High-Speed Burst Mode	Alternate Low-Power
	Dp-Line	Dn-Line		
HS-0	HS Low	HS High	Differential-0	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 2
ALP-00	ALP Low	ALP Low	N/A	Stop or ULPS State
ALP-01	ALP Low	ALP High	N/A	Wake
ALP-10	ALP High	ALP Low	N/A	End of Burst

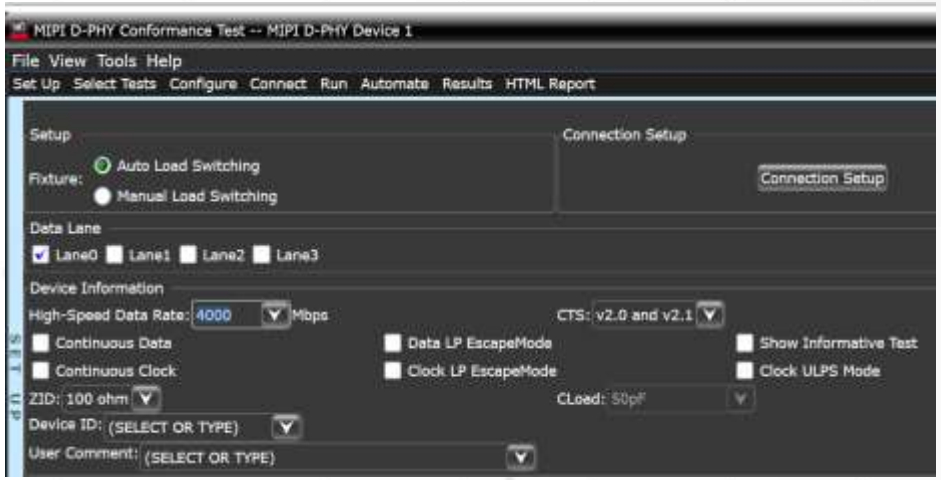
New D-PHY eye diagram test on D-PHY v3.0

DATA EYE DIAGRAM ESTIMATION

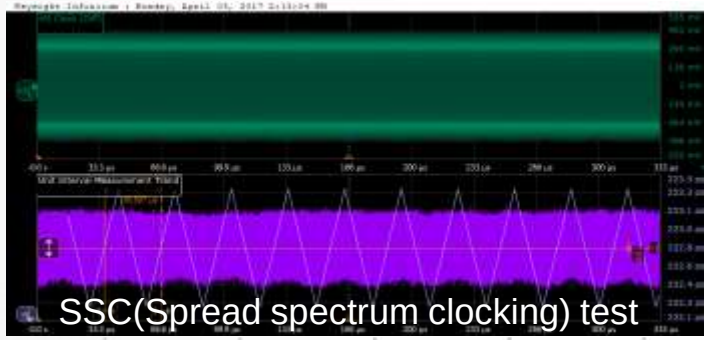


MIPI D-PHY TX solution

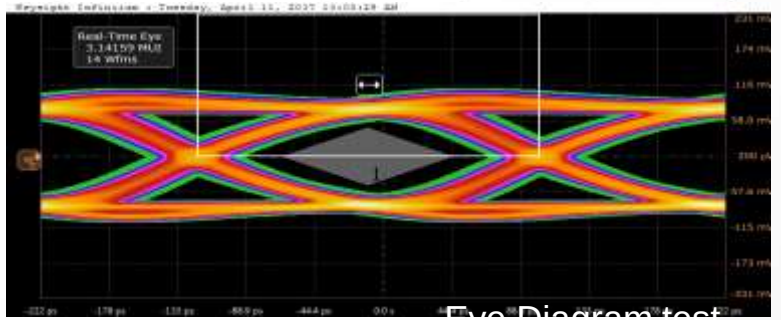
Keysight UXR digital oscilloscope D9020DPHC
MIPI D-PHY compliance software



- ✓ Industry first supporting D-PHY v2.0/v2.1 specification test
- ✓ Already proven solution with key industry leading customers
- ✓ Reference channel embedding supporting
- ✓ It is supporting of DPHY app to newer high-end UXR scope

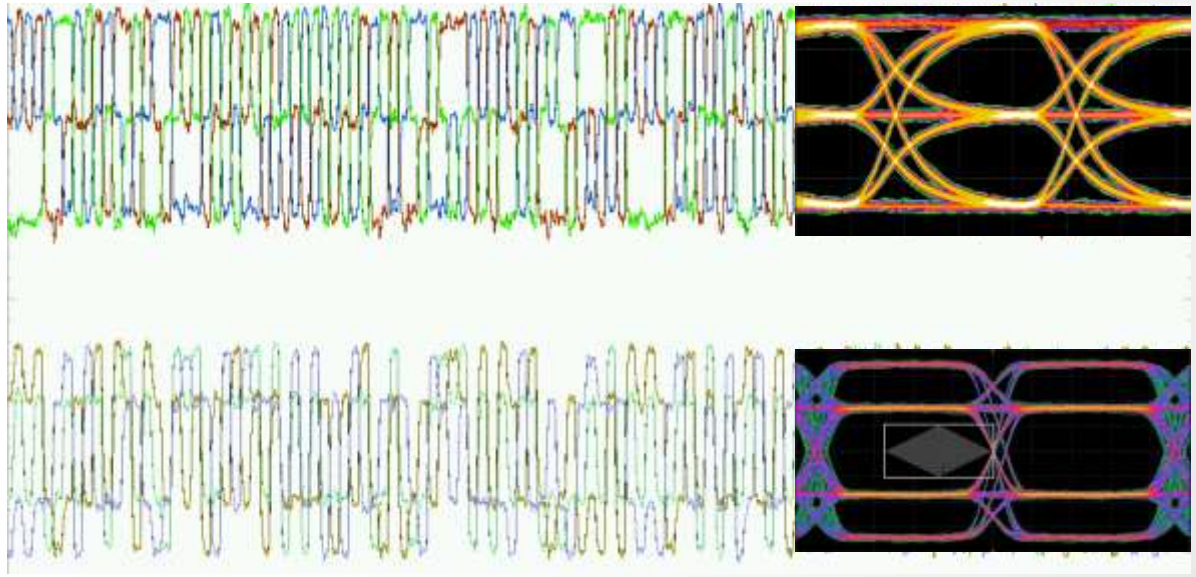


SSC(Spread spectrum clocking) test



Eye Diagram test

CPHY updating and solution



C-PHY Specification update

C-PHY V2. IS APPROVED

C-PHY 1.2 : Approved Mar 28, 2016

C-PHY 2.0 : Approved Sep 9, 2019

- Speed up to 6Gsps~8Gsps
- RX Equalizer (1st order CTLE)
- Fast bus turn around

C-PHY Specification update

C-PHY V2.1 IS APPROVED

C-PHY 2.0 : Approved Sep 9, 2019

C-PHY 2.1 : Approved July 21, 2021

- Package model apply to Eye diagram >=3.5G
- Minor updates

C-PHY CTS updates

NO C-PHY V1.2 CTS

CTS 1.1 : Approved May 21, 2019

C-PHY 2.0 : revision 03, April, 20, 2020

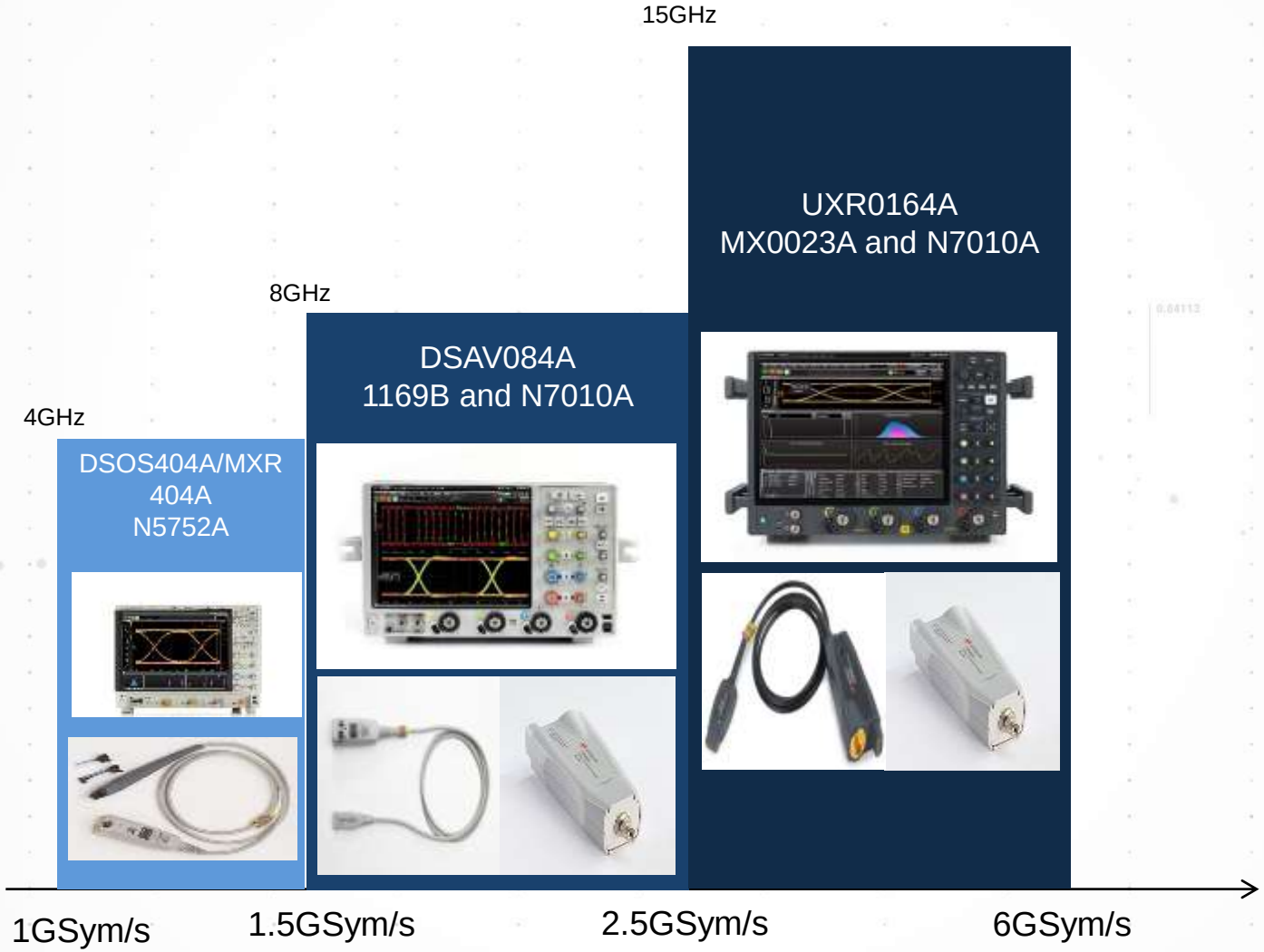
- Oscilloscope bandwidth updates
- Direct connect test for VOHHS and VCPTX
- Reduced amplitude LVHS(Test 1.2.7, 1.2.10)
- LVLP operation(Test 1.1.1)
- Removed DeltaUI(Test 1.2.20)
- Eye diagram test with Adv RX EQ(Test 1.2.21)
- UI Jitter Peak(Test 1.2.22)
- Calibration Preamble sequence (Group 1.5.x) (informative)

New bandwidth requirement

OSCILLOSCOPE BANDWIDTH

- Use same method, 5th harmonic term
- 6Gbps(Standard channel)
  - Fundamental frequency = 3GHz
  - 5th harmonic = 3 x 5 = 15GHz
- 8Gsps (Short channel)
  - Fundamental frequency = 4GHz
  - 5th harmonic = 4 x 5 = 20GHz

Keysight Solutions for MIPI C-PHY TX PHY-test



LVHS(Low Voltage High Speed)

REUSE D-PHY DRIVER IN C-PHY

Parameter	Description	Min	Nom	Max	Units	Notes
$\|V_{OD}\|$ strong	HS transmit differential voltage of the differential strong one and strong zero specified in ***Table 37***.	–	–	300	mV	1
$\|V_{OD}\|$ weak	HS transmit differential voltage of the differential weak one and weak zero specified in ***Table 37***.	90	–	–	mV	1, 4
$\|V_{OD}\|$ Weak (LVHS)	HS transmit differential voltage of the differential weak one and weak zero specified in ***Table 37***, Low-Voltage High-Speed Mode.	70	–	–	mV	1

Note:

1. *Value when driving into load impedance, Z_{ID}, equal to 100 Ω.*
2. *A transmitter should minimize ΔV_{OD} and $\Delta V_{CPTX(HS)}$ to minimize radiation and optimize signal integrity.*
3. *The nominal value of V_{CPTX} should be in the specified range depending upon the supply voltage used for each implementation.*
4. *The Transmitter should meet the \|VOD\| weak minimum level, but this is not required. Meeting the \|VOD\| weak minimum specification will not guarantee that the eye opening in **Section 10.3.1** is met. It is a requirement for the transmitter to meet the Tx Timing Specification requirements of **Section 10.3.1**.*

Figure 1.2.7-1: V_{OD} Specification Conformance Requirements

If DUT supports LVHS, which expected to use slightly low voltage than normal C-PHY HS swing voltage. VOD Weak minimum voltage limit should be less than normal voltage. (90mV->70mV)

The measurement will be performed for the $V_{OD\_AB} = V_A - V_B$, $V_{OD\_BC} = V_B - V_C$, and $V_{OD\_CA} = V_C - V_A$ signals, and the Strong 1, Weak 1, Weak 0, and Strong 0 average (mean) values will be measured for each.

For all 3 differential pairs and all Lanes, the average (mean) Strong 1 V_{OD} value must be less than 300 mV to be considered conformant. The average (mean) Weak 1 V_{OD} value must be greater than 90 mV or the average (mean) Weak 1 (LVHS) V_{OD} value must be greater than 70 mV if DUT supports low voltage high speed (LVHS) to be considered conformant. The average (mean) Weak 0 V_{OD} value must be less than -90 mV or the average (mean) Weak 0 (LVHS) V_{OD} value must be less than -70 mV if DUT supports low voltage high speed (LVHS) to be considered conformant. The average (mean) Strong 0 V_{OD} value must be greater than -300 mV to be considered conformant.

LVLP(Low Voltage Low Power)

REDUCE MAXIMUM SWING FOR LP

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevenin output high level	0.95	–	1.3	V	–
		0.95	–	1.1	V	3

Note:

3. Applicable when the Lane Module is in optional LVLP operation.

Figure 1.1.1-1: V_{OH} Specification Conformance Limits

Also, to reduce measurement noise, a 400-MHz, 4th-order Butterworth lowpass test filter is applied to the source waveform for this measurement. (See Test 1.1.5 Discussion for details.)

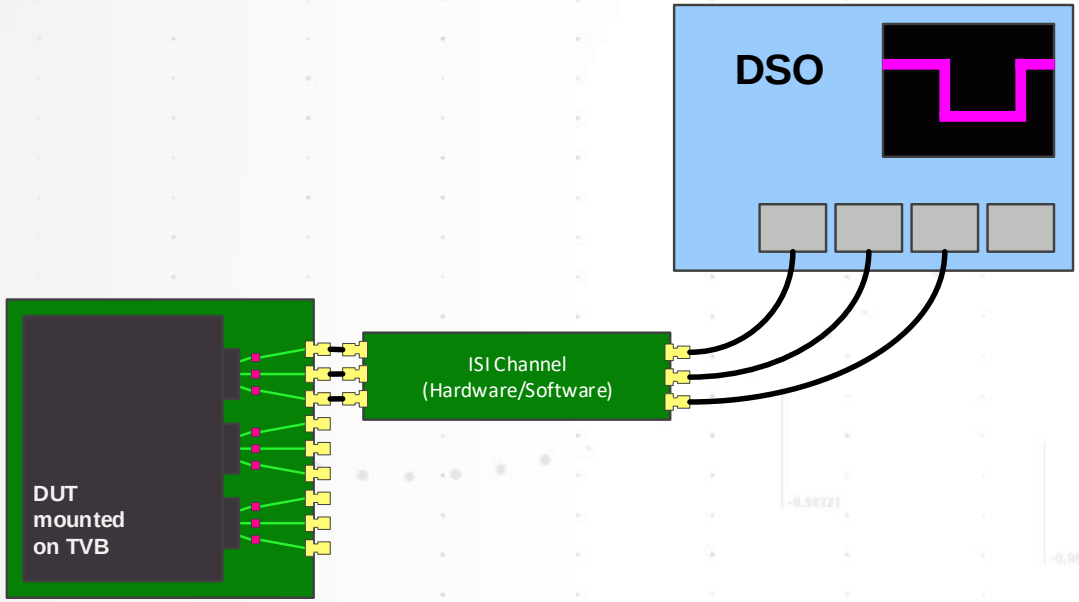
For all Lanes, the value of V_{OH} for the V_A, V_B, and V_C signals have to be between 0.95 V and 1.3 V to be considered conformant [2]. In the optional LVLP operation, the value of V_{OH} for the V_A, V_B, and V_C signals have to be between 0.95 V and 1.1 V to be conformant [2].

To support single nano meter process, MIPI reduced maximum Low Power swing voltage from 1.3V to 1.1V, Minimum limit is same.

Tx Eye diagram test condition changes

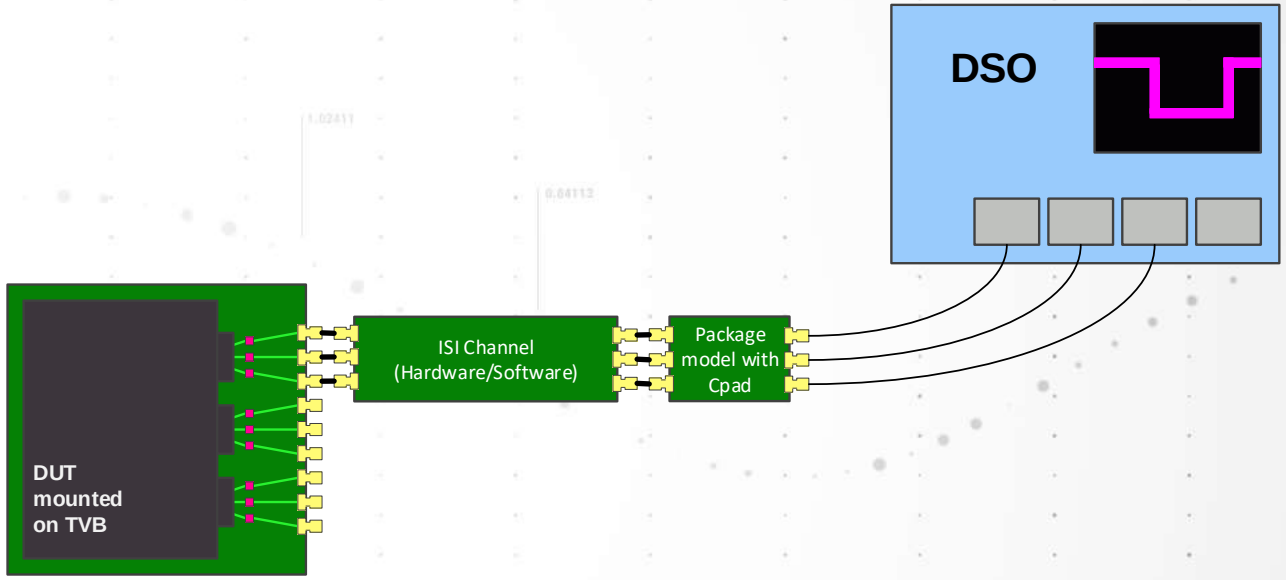
ADD PKG AND CPAD IN CHANNEL

C-PHY v1.1/1.2



TX : Advance Tx EQ on (optional)
ISI : Standard channel
RX : None

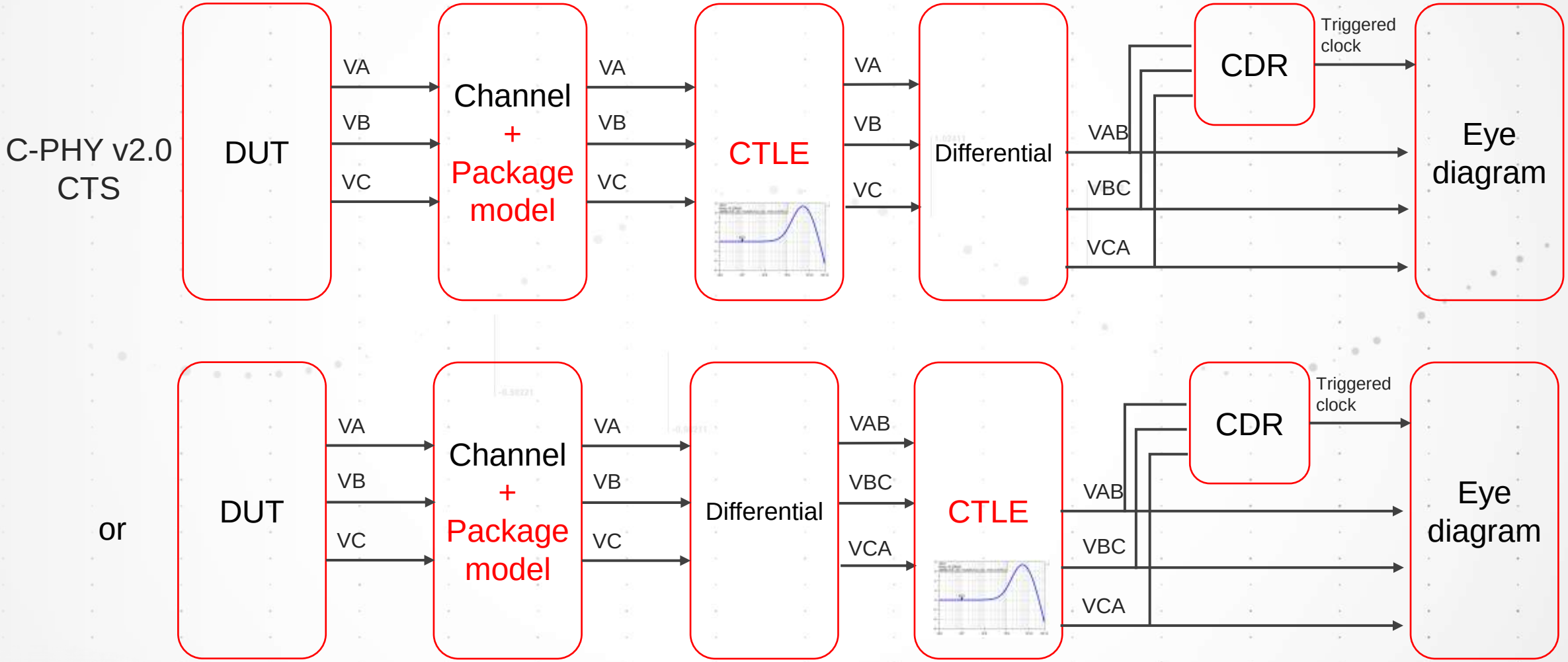
C-PHY v2.0



TX : Advance Tx EQ off (mandatory)
ISI : new Standard channel + Package model with Rx C_{PAD}
RX : CTLE (continuous time linear equalizer)

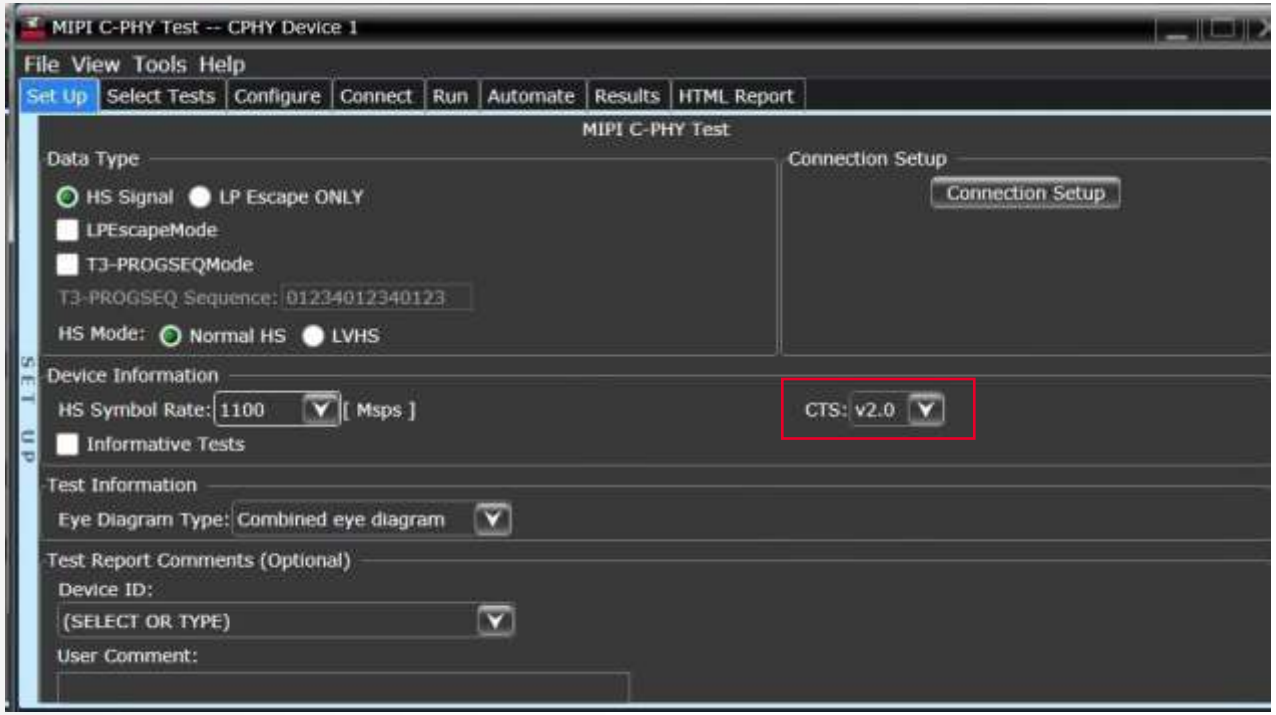
New clock recovery process on eye diagram test

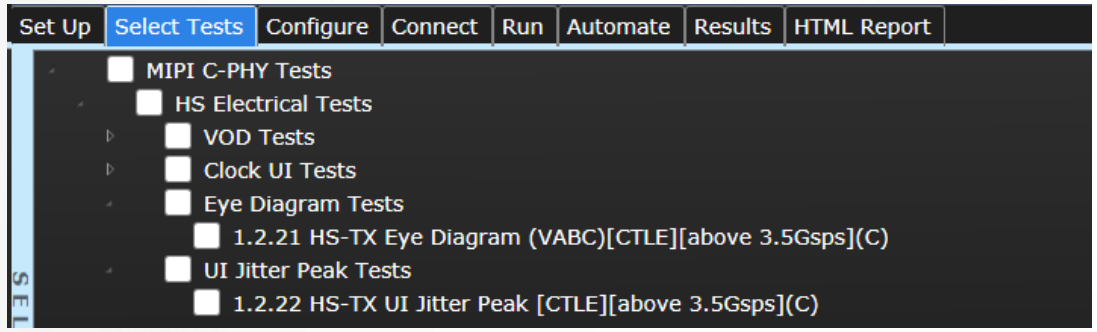
CTLE APPLIED BEFORE CDR



D9010CPHC C-PHY TX test solution

CPHY2.0 CTS

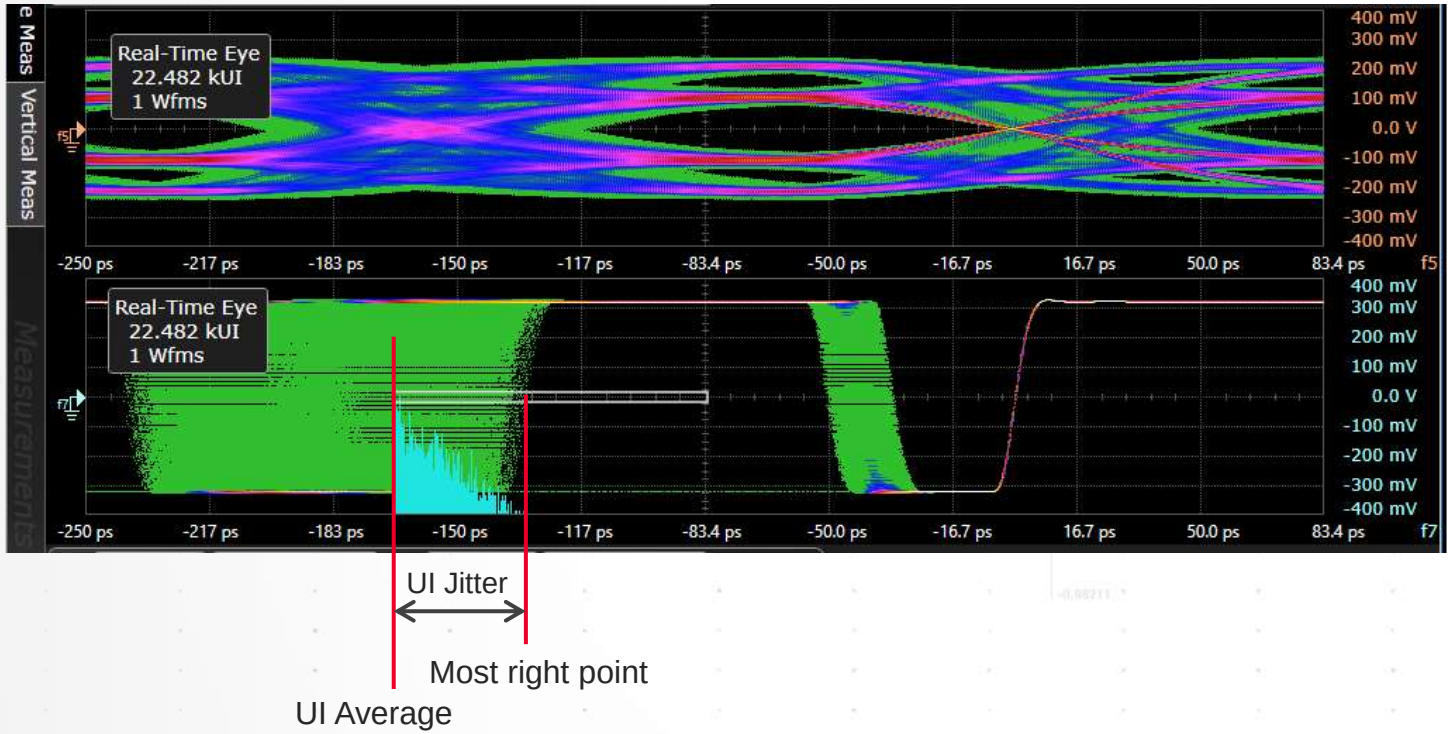




- It needs new D9010CPHC license to enable C-PHY v2.0 CTS items. Older U7250A license won't work for this new CTS version.
- Also need Equalization(D9020ASIA) option for C-PHY v2.0 Eye diagram and UI Jitter test. **It is okay to use C-PHY v1.1 test items without Equalization option but the app pops up warning.**

UI Jitter Peak

NEW TEST

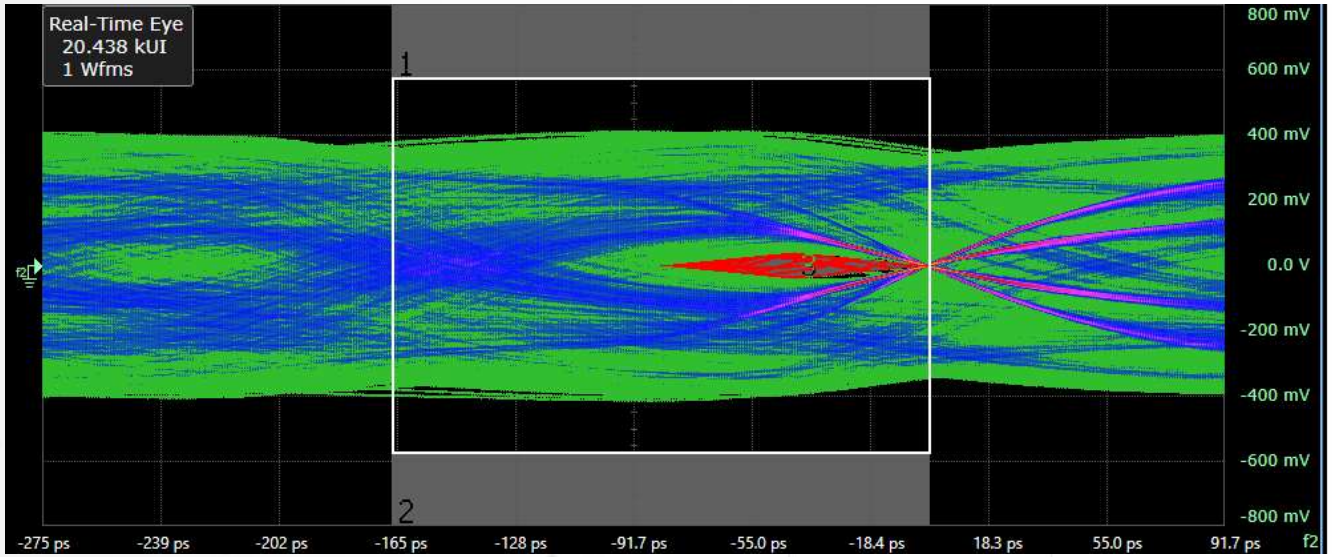


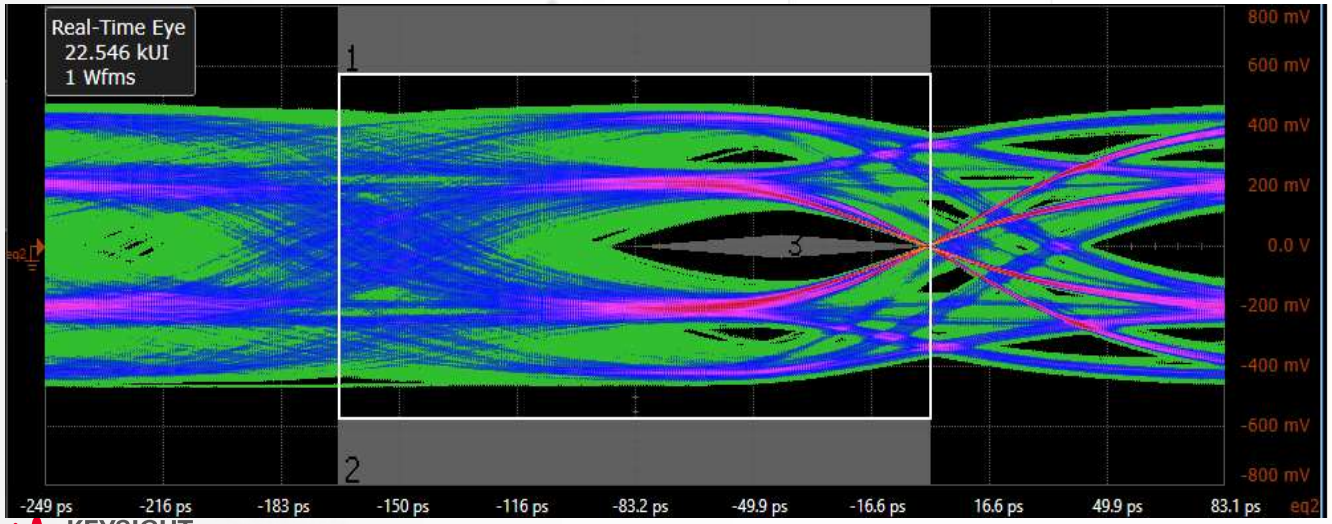
Meet eye diagram result along with UI Jitter peak, UI Jitter peak test will reuse Eye diagram test's CTLE parameter for the DUT that runs above 3.5Gsps and up to 6Gsps

Above 6Gsps, Short channel can be used for optionally.

CTLE(Continuous Time Linear Equalizer)

WHERE TO PUT IN

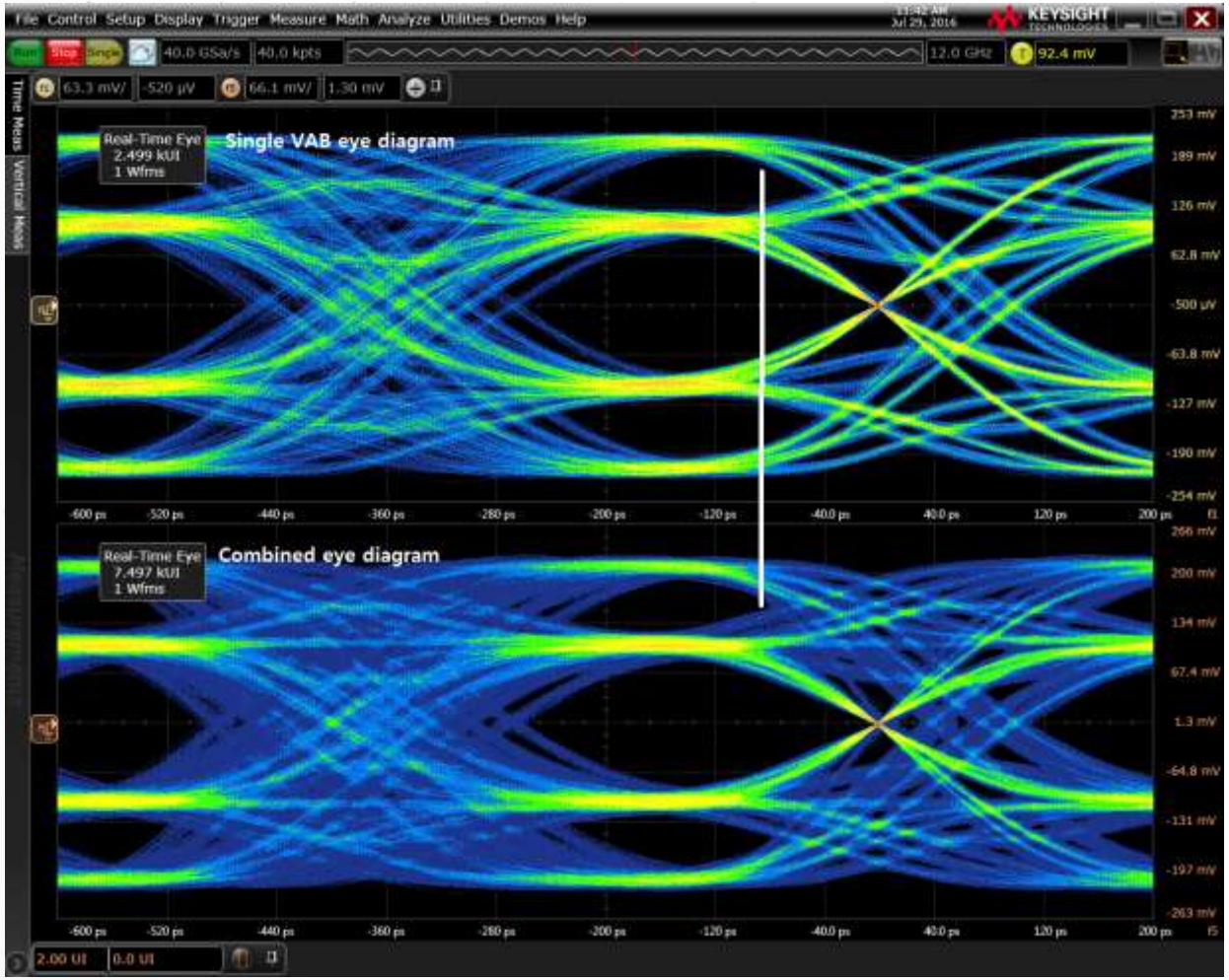




Just add Channel + Package effects on 6Gsps

Apply CTLE first and add channel result

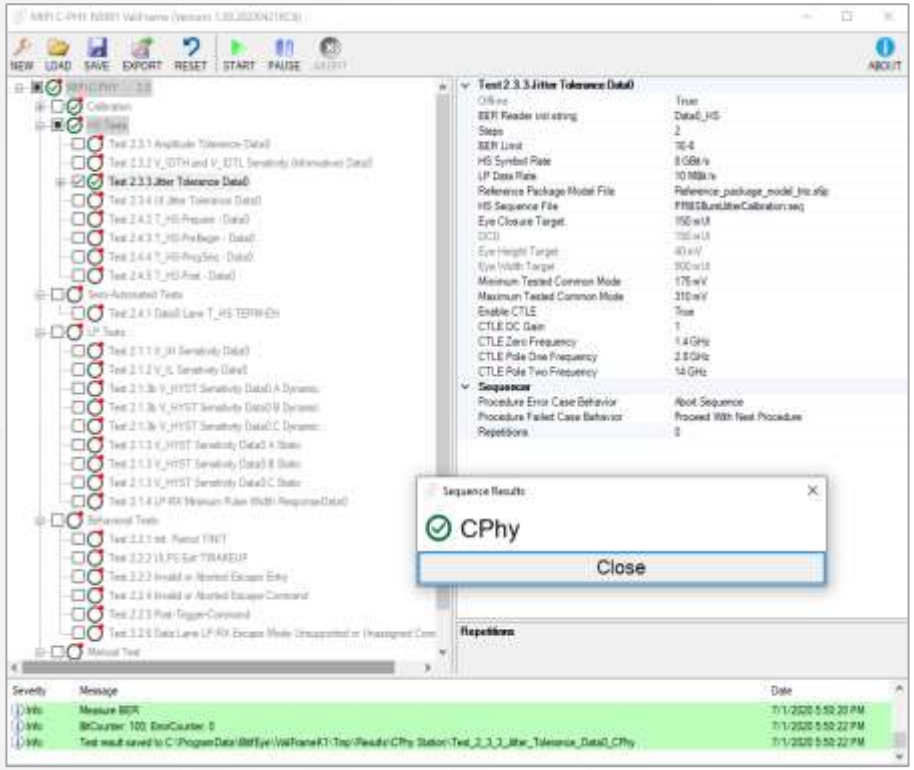
Combinded 3 waveforms to 1 eye diagram

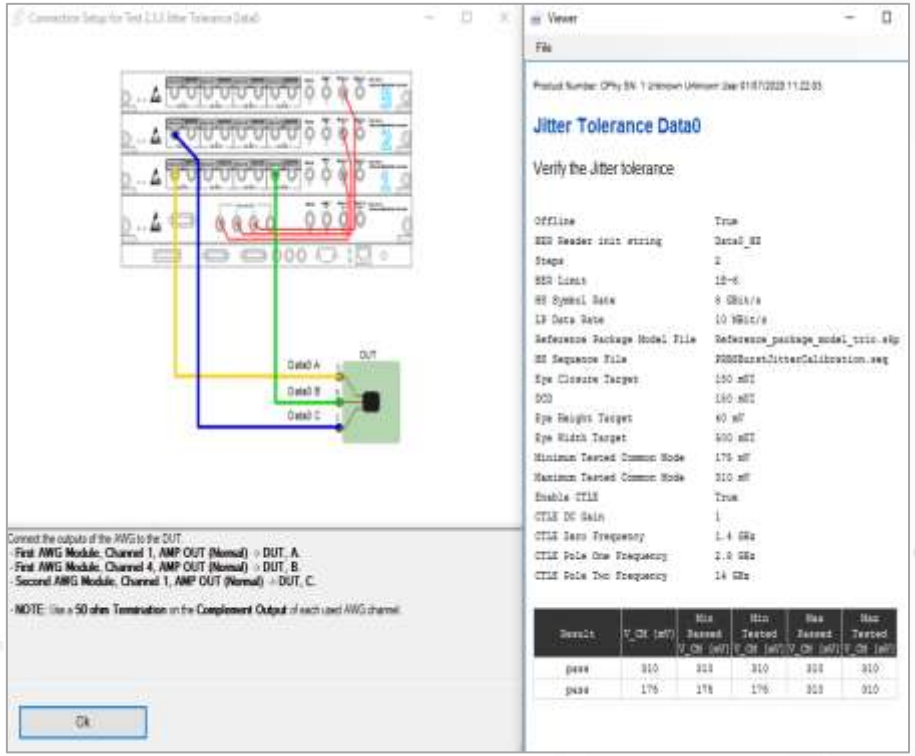


Result show that eye shape is not same

N5991MC2A MIPI C-PHY v2.0 Receiver test

C-PHY V2.0 SUPPORTS

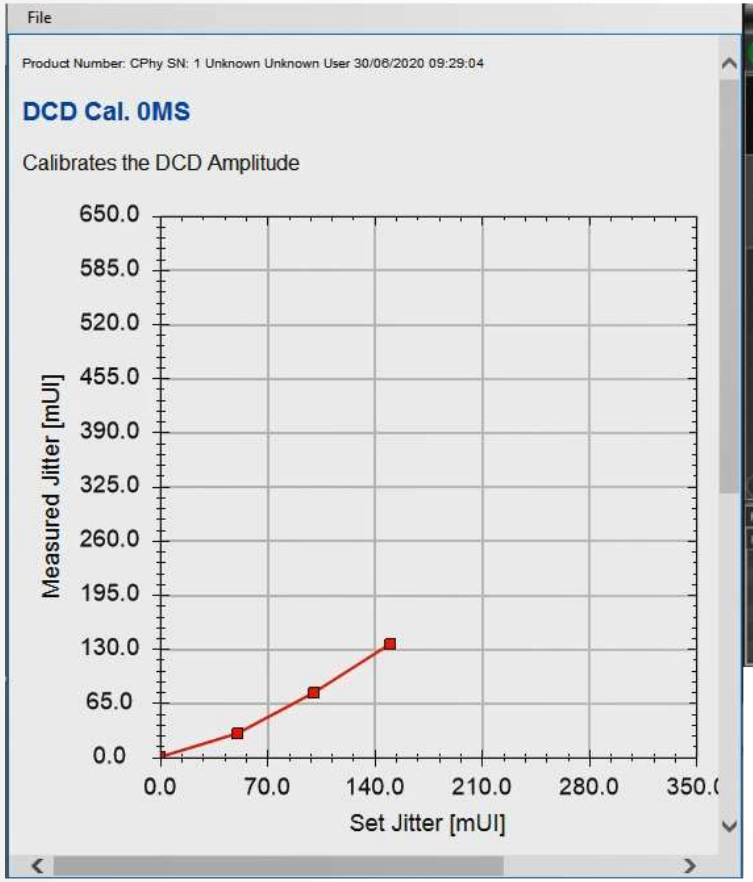


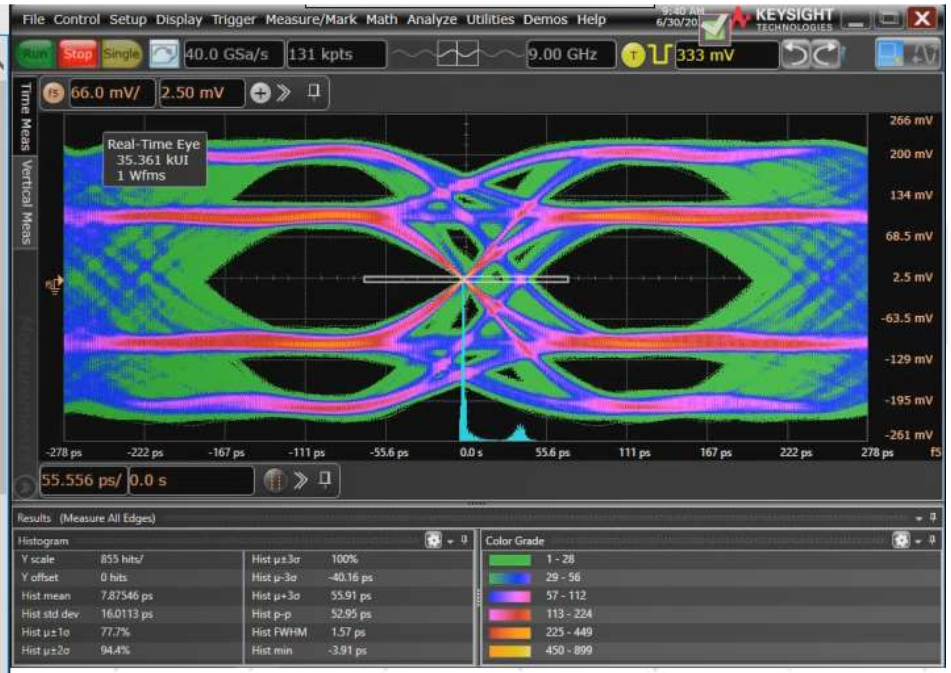


- Industry first and only solution that supports C-PHY v2.0 CTS
- Clear connection instruction for fast setup
- Test result viewer
  - Individual test result
  - Or export a complete calibration and test report

N5991MC2A MIPI C-PHY v2.0 Receiver test

C-PHY V2.0 SUPPORTS

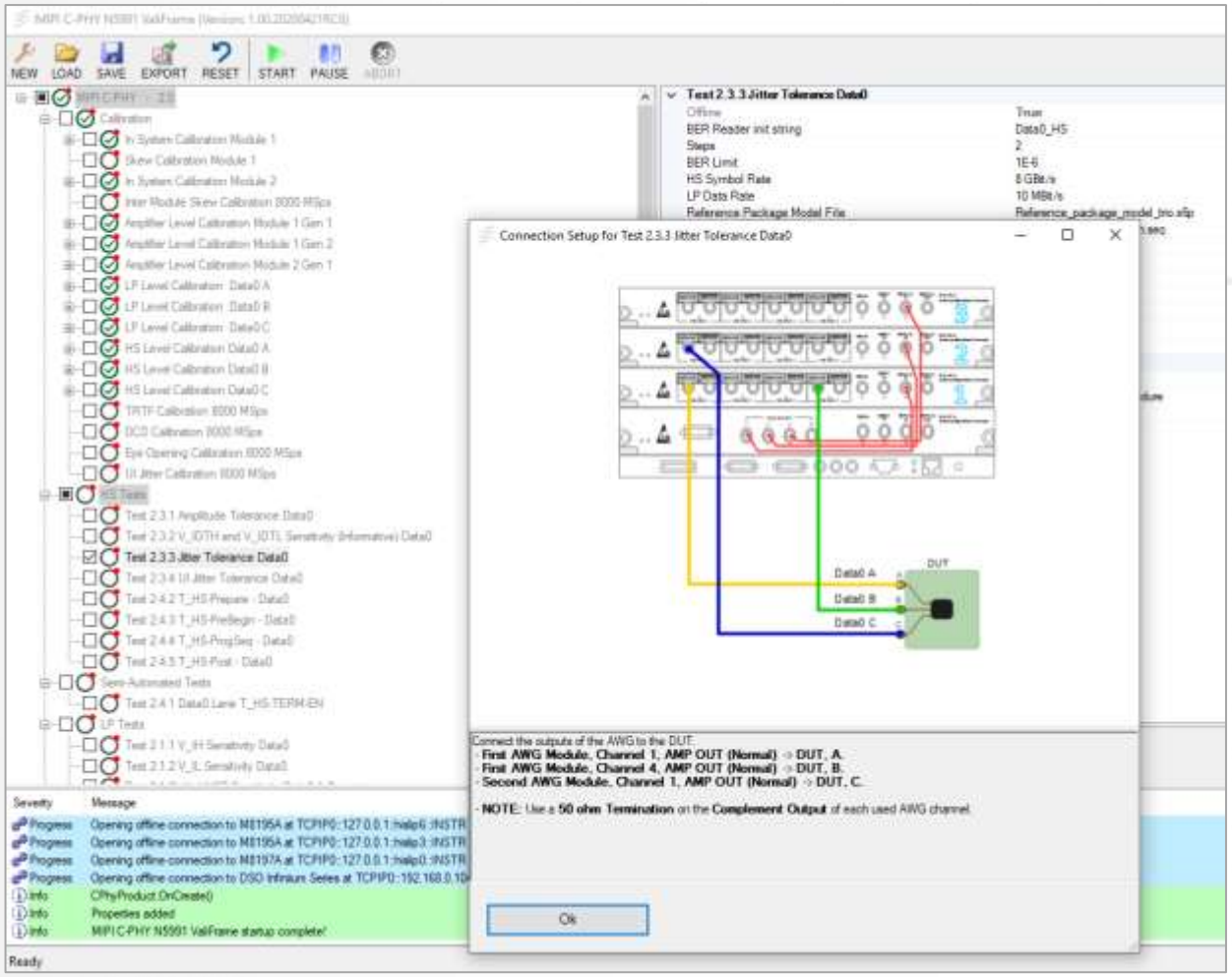




- Upgraded calibration with C-PHY triggered eye from oscilloscope
  - Rise time
  - DCD
  - Eye diagram
  - UI

N5991MC2A MIPI C-PHY v2.0 Receiver test

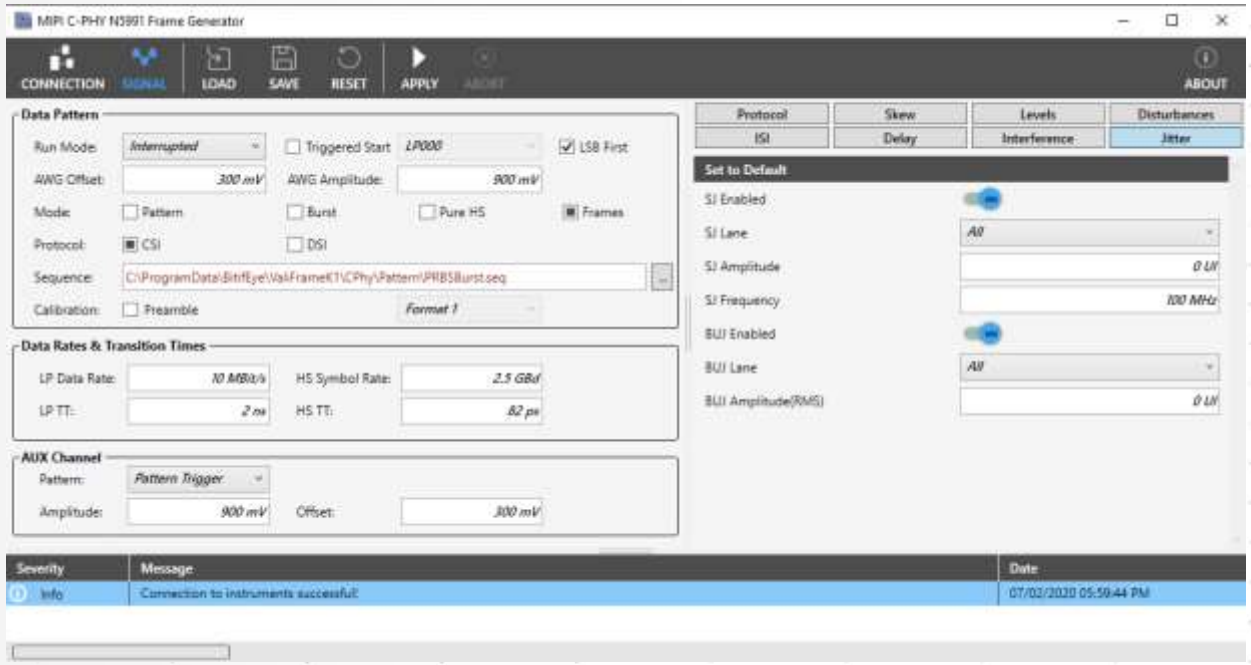
C-PHY V2.0 SUPPORTS



- **2 AWG** can generate up to **9Gsps symbol rate**
- Each channel have **32Gsa/s sampling**
- **N5991MCHZ-ADD** license required

N5991MC2E MIPI C-PHY v2.0 Frame Generator

SIGNAL GENERATION TOOL



- Intuitive GUI based C-PHY signal generation
- Simply control C-PHY electrical and timing parameters

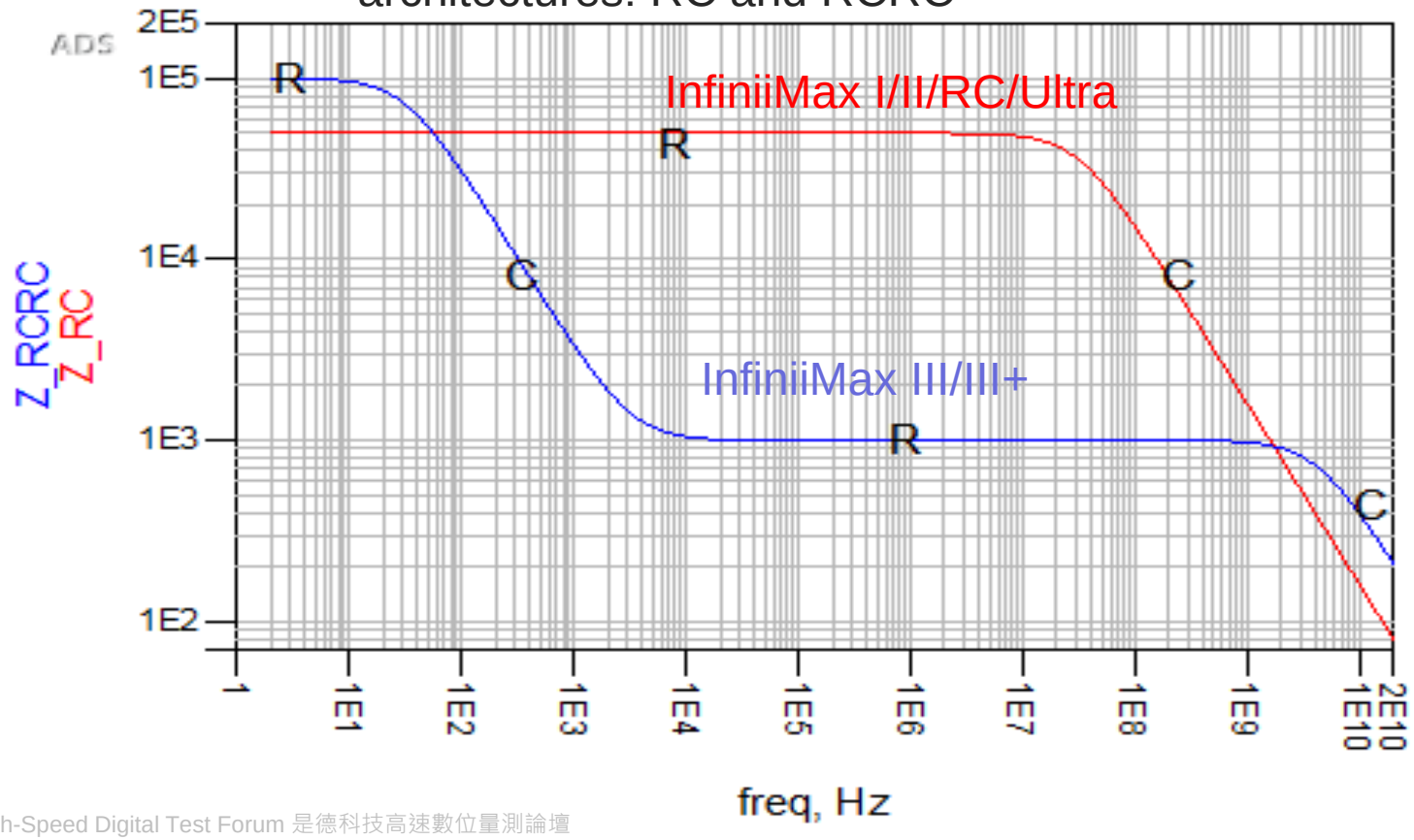
Probing with MIPI signal

Probe Loading Basics

INPUT IMPEDANCE VARIES ACROSS FREQUENCY

- **RC architecture** (InfiniiMax I/II/RC/Ultra)
  - Best for measuring signals that transition to low power modes
  - highest impedance (lowest loading, least signal distortion) across the widest frequency range
- **RCRC architecture** (InfiniiMax III/+)
  - Best when higher bandwidth is necessary, or signals have low source impedance
  - Probe loading can affect the circuit under test

Input impedance profile of two common probe architectures: RC and RCRC



Keysight InfiniiMax Ultra Probes

GET CLOSER TO THE TRUTH

- Launching September 1, 2021
- **Highest accuracy** differential probe family for all high-speed digital engineers
- From **4 to 25 GHz bandwidth**
- **Lowest loading**
- **Lowest noise**
- **Least signal distortion**
- **Best solution** to probe small devices

KEYSIGHT
TECHNOLOGIES